DV/DT Immunity Improved in Synchronous Buck Converters

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Controlling dv/dt-induced turn-on effect can increase overall converter efficiency and MOSFET reliability.

As nonisolated synchronous buck power converters continue pursuing higher switching frequencies, the key limiting factor has become switching losses in the high-side MOSFET. The faster the high-side MOSFET can transition on and off, the lower the associated switching losses become. However, addressing one problem introduces another. Specifically, the faster the high-side MOSFET is turned on, the more susceptible the low-side synchronous MOSFET becomes to dv/dt-induced turn-on.

Dv/dt turn-on establishes a situation where the synchronous MOSFET can momentarily become turned on, even though the gate-drive signal commands it to be turned off. In a synchronous buck power converter, when the high-side MOSFET is on, the low side must be off. Inadvertently turning on the synchronous MOSFET through dv/dt can result in shoot-through current when the high-side and low-side MOSFETs momentarily conduct simultaneously. In most cases, the converter will operate as expected with little noticeable difference in performance. However, when the applied dv/dt results in a gate voltage that exceeds the MOSFET gate-to-source threshold voltage, the converter's reliability and overall efficiency suffers.

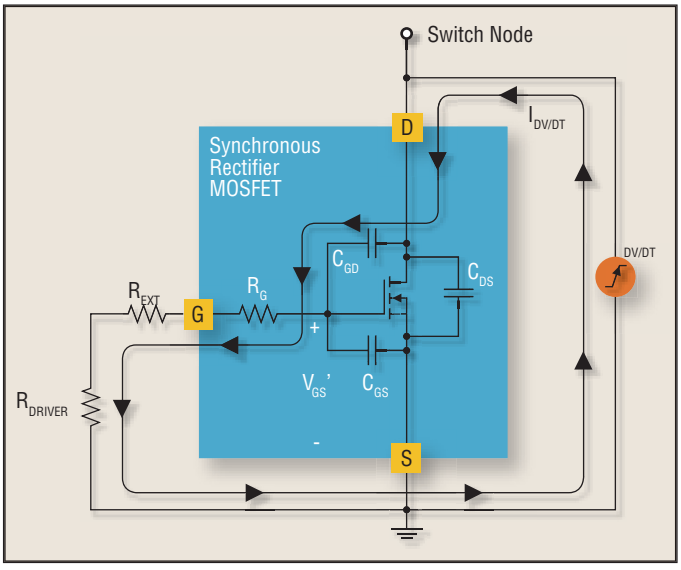

Fig. 1. *Turn-on of the high-side MOSFET (not shown) produces a voltage transient dv/dt across the low-side (synchronous) MOSFET, which leads to the off-state current conduction shown here.*

Although the source of the problem resides internally in the MOSFET, there are design steps that can make the synchronous MOSFET less susceptible to dv/dt-induced turn-on. Since each application can vary (high frequency, low voltage, high current, etc.), the solutions for each application are unique and deserve careful consideration.

Fig. 1 shows a low-side MOSFET (off state) of a synchronous buck converter at the moment a positive dv/dt transition appears across the drain-to-source junction. When the high-side switch turns on, the voltage across the drain-to-source of the low-side synchronous MOSFET rapidly increases, producing a fast-change in voltage, dv, within a very short time interval, dt.

The applied dv/dt results in an instantaneous current flow through the charge of the MOSFET parasitic drain-to-gate capacitance (C_{GD}). For $dt/C_{GS} >> R_G + R_{EXT} + R_{DRIVER}$, most of the current through C_{GD} would ideally flow out of the gate terminal and back through the driver sink resistance as shown in **Fig. 1**. The current flowing through the internal gate resistance (R_G) produces a spurious voltage spike (V_{GS}') seen at the MOSFET gate, which can be approximated by this equation:

$$V_{GS}' \approx (R_G + R_{EXT} + R_{DRIVER}) \times C_{GD} \times \frac{dv}{dt} \qquad \text{(Eq. 1)}$$

If V_{GS}' is less than the turn-on threshold voltage ($V_{GS(TH)}$), then the MOSFET will not turn on. Therefore, the design goal should not be to completely eliminate the effect of V_{GS}' but to minimize it to a maximum value less than $V_{GS(TH)}$ under

all conditions as stated in the following equation:

$$(R_G + R_{EXT} + R_{DRIVER}) \times C_{GD} \times \frac{dv}{dt} < V_{GS(TH)} \quad \text{(Eq. 2)}$$

Note that there are several approaches for satisfying Eq. 2. R_G, C_{GD} and R_{DRIVER} are component parameters that the designer has no control over. R_{EXT} and dv/dt tend to be more easily addressed since they are design-dependant variables. The first step in designing a synchronous buck power stage for maximum dv/dt immunity begins with proper component selection.

Synchronous Rectifier MOSFET Selection

The first intuitive solution might be to select a MOSFET with a higher turn-on threshold voltage. This makes the MOSFET more immune to dv/dt-induced turn-on, as evident in Eq. 2. However, since synchronous rectifier MOSFETs often carry high-load currents at low duty cycle, selecting the lowest on-resistance device is a primary concern. Since MOSFETs with higher turn-on thresholds also have higher associated on-resistance, this is not the best starting point.

MOSFETs suitable for synchronous rectifier applications are sometimes specified as having improved Cdv/dt-induced turn-on immunity. Aside from package type, voltage rating and current rating, MOSFETs are typically selected for their on-resistance and gate-charge characteristics. So, what does it mean to select a device that is robustly designed for dv/dt turn-on immunity?

The natural dv/dt limit of a MOSFET is defined by how much dv/dt can appear across the drain-to-source without inducing a gate-to-source voltage exceeding $V_{GS(TH)}$. By considering the capacitive divider formed between C_{GD} and C_{GS} shown in **Fig. 1** (when the MOSFET is out of circuit), the dv/dt-induced gate-to-source voltage can be calculated by this equation:

$$V_{GS}' = \left\{ \left(\frac{C_{GD}}{C_{GD} + C_{GS}} \right) \times V_{DS} \right\} < V_{GS(TH)} \quad \text{(Eq. 3)}$$

As long as $V_{GS} < V_{GS(TH)}$, the MOSFET will remain off. From Eq. 3, it is obvious that lowering C_{GD} and increasing C_{GS} will result in better dv/dt immunity. However, these are nonlinear parameters, internal to the MOSFET that the power supply designer has no control over. Since MOSFETs are selected based upon gate-charge requirements, Eq. 3 can be rewritten as Eq. 4 to establish an expression related to charge, as in Eq. 5, instead of capacitance:

$$C_{GD} \times (V_{DS} - V_{GS(TH)}) < C_{GS} \times V_{GS(TH)} \quad \text{(Eq. 4)}$$

Dividing both sides of Eq. 4 by the right side of the equation gives Eq. 5:

$$\frac{Q_{GD}}{Q_{GS(TH)}} = \left\{ \frac{C_{GD} \times (V_{DS} - V_{GS(TH)})}{C_{GS} \times V_{GS(TH)}} \right\} < 1 \quad \text{(Eq. 5)}$$

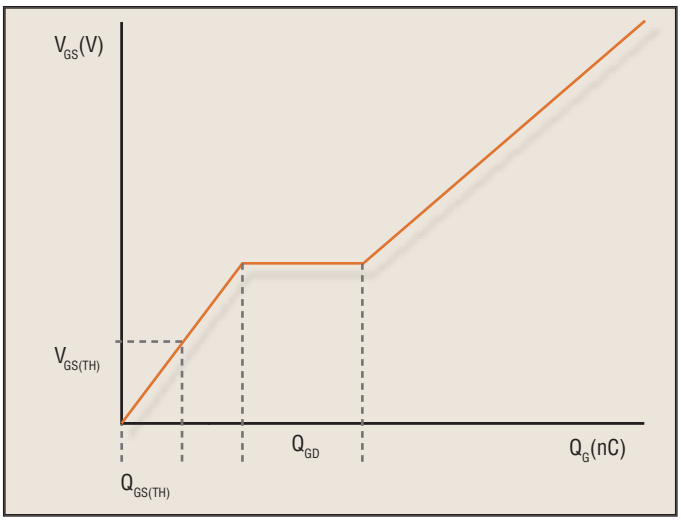

Fig. 2. *$Q_{GS(TH)}$ and Q_{GD} may be determined from the MOSFET gate-charge curve.*

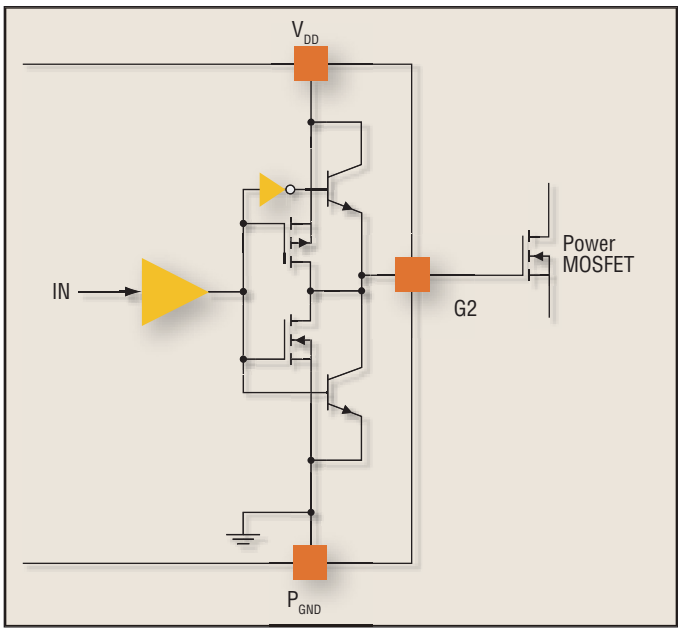

Fig. 3. *The TrueDrive gate-drive architecture (low-side only) from Texas Instruments places bipolar and MOS transistors in parallel to deliver the rated drive current while lowering the pull-down impedance for better dv/dt immunity.*

$Q_{GS(TH)}$ is the gate-to-source charge for $0\ V < V_{GS} < V_{GS(TH)}$ and Q_{GD} is the gate-to-drain charge defined at the Miller plateau shown in **Fig. 2**.

The expression of Eq. 5 states that the ratio of charge between Q_{GD} and $Q_{GS(TH)}$ should be less than 1 to prevent dv/dt-induced turn-on. However, there are two problems with this approach. Synchronous MOSFETs are selected primarily based upon lowest on-resistance, so the $Q_{GD}/Q_{GS(TH)}$ criteria should be secondary when conduction losses are considered. Secondly, from Eq. 5 it can be seen that as V_{DS} increases, $Q_{GD}/Q_{GS(TH)}$ also increases. For a synchronous buck converter, V_{DS} is equal to V_{IN} when the high-side MOSFET is conducting. Therefore, converters operating from a higher-input voltage become more susceptible to dv/dt-induced turn-on, even when the synchronous MOSFET is selected according to Eq. 5. Nonetheless, from a dv/dt immunity point of view, this a good starting point to keep in mind, especially for low-voltage converters.

Whether the MOSFET gate-drive circuitry is internal to a dc-dc controller or external, there are specific considerations that can improve dv/dt immunity.

MOSFET Driver Selection

Whether the MOSFET gate-drive circuitry is internal to a dc-dc controller or external, such as a stand-alone synchronous buck MOSFET driver IC, there are specific considerations that can improve dv/dt immunity.

Earlier, MOSFET drivers were designed using a complementary bipolar process to deliver the high current required to efficiently switch the power MOSFET. These types of drivers are effective at sourcing high current, but their ability to fully hold the power MOSFET in a low state is limited by their saturation voltage. Some bipolar drive stages can have saturation voltages as high as 0.75 V. For a synchronous MOSFET with an arbitrary threshold voltage of 1.25 V, this would only leave 0.5 V of dv/dt headroom before cross-conduction could begin.

Most modern synchronous MOSFET drive stages use a MOS-only output stage. ICs using MOS-only drive stages overcome the drawbacks of bipolar stages by fully switching the power MOSFET to ground during the off state. This provides an added benefit for the dv/dt problem, but the disadvantage of a MOS-only driver stage is its inability to source high-gate current at low voltage, such as the power MOSFET gate-to-source threshold voltage.

Why sacrifice drive current for better dv/dt immunity? As shown in **Fig. 3**, a combination bipolar and MOS architecture, such as that provided by the TrueDrive technology from Texas Instruments, offers the benefits of each process.

The bipolar section provides the rated driver current where it is needed most: at the power MOSFET's Miller plateau. The MOS section is placed in parallel with each bipolar device, yielding a lower pull-down impedance for better dv/dt immunity. For driving low on-resistance MOSFETs with low gate-to-source turn-on thresholds, in applications where the possibility of dv/dt turn-on is a concern, a MOS/bipolar drive stage can offer significant performance improvements. When combined with a

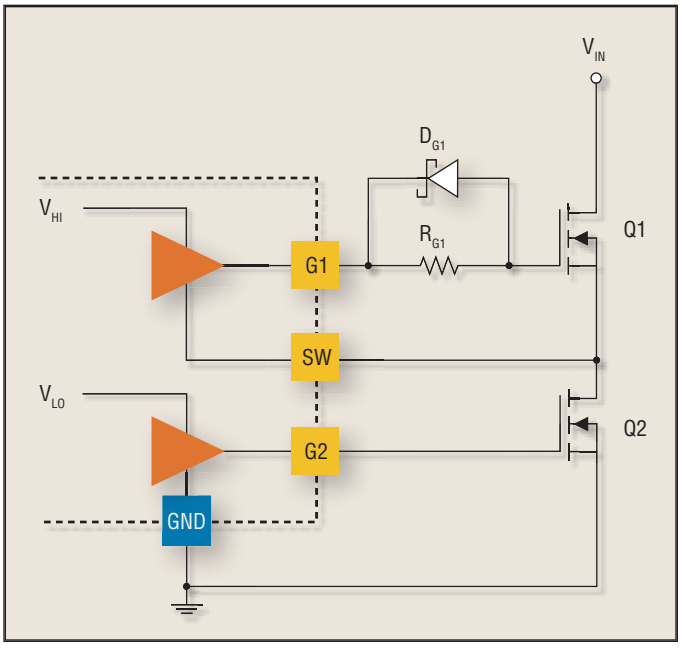

Fig. 4. *Placing a Schottky diode (D_{G1}) in parallel with an external gate resistor (R_{G1}) slows down the turn-on of the high-side MOSFET.*

MOSFET selected according to Eq. 5, this can sometimes be all the dv/dt precaution that is necessary for low-voltage synchronous buck converters.

Gate-Drive Considerations

In addition to MOSFET selection and drive-stage considerations, there are circuit design measures that should be reviewed. One technique is to slow down the turn-on of the high-side MOSFET, effectively increasing the dt component of Eq. 2. The simplest way to achieve this is to place a Schottky diode in parallel with an external gate resistor (**Fig. 4**). The rising edge (turn-on) of Q1 now can be controlled by R_{G1}, while the falling edge (turn-off) is

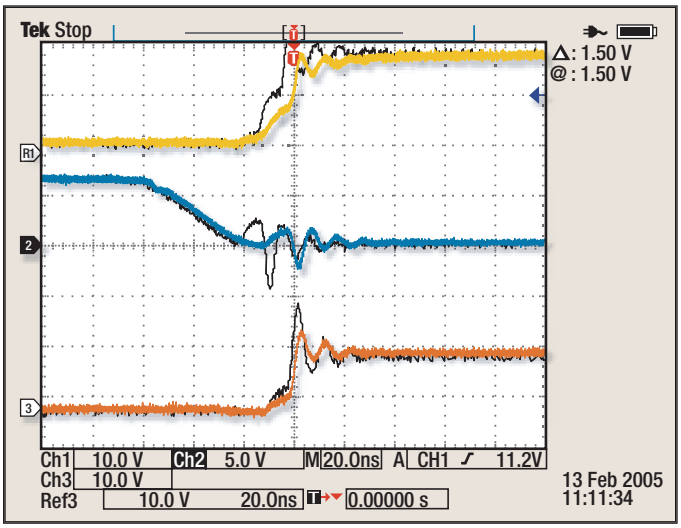

Fig. 6. *A 12-V input, 1.8-V output synchronous buck converter driven by a UCC27223 with an external high-side boost, gate-drive configuration produces the waveforms shown here for the cases R_{HI} = 0 Ω (V_{GS}(dv/dt) = 2.6 V) and R_{HI} = 5.11 Ω(V_{GS}(dv/dt) = 1.5 V).*

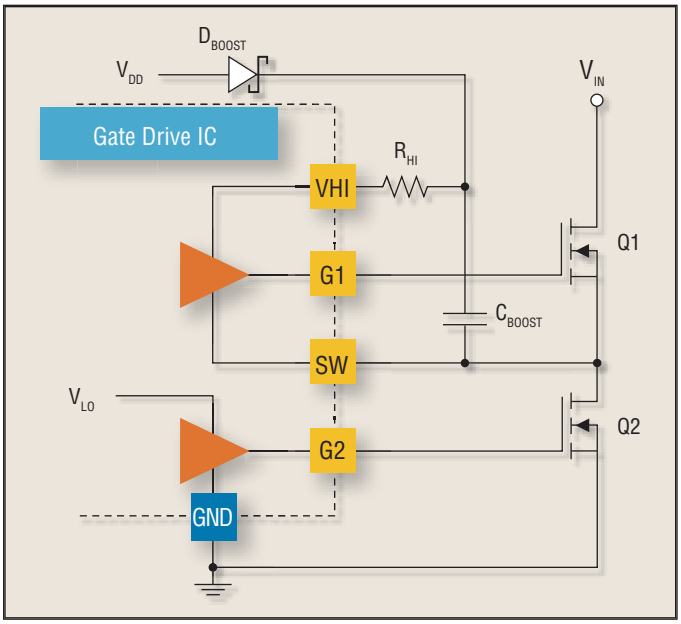

Fig. 5. *For circuits with external high-side supply boost, a small resistor (R_{HI}) can slow down the turn-on of the high-side MOSFET .*

unaffected since R_{G1} is shorted by D_{G1} when the drive stage is sinking current.

Fig. 5 illustrates a synchronous drive stage that uses an external boost circuit to develop the high-side gate drive.

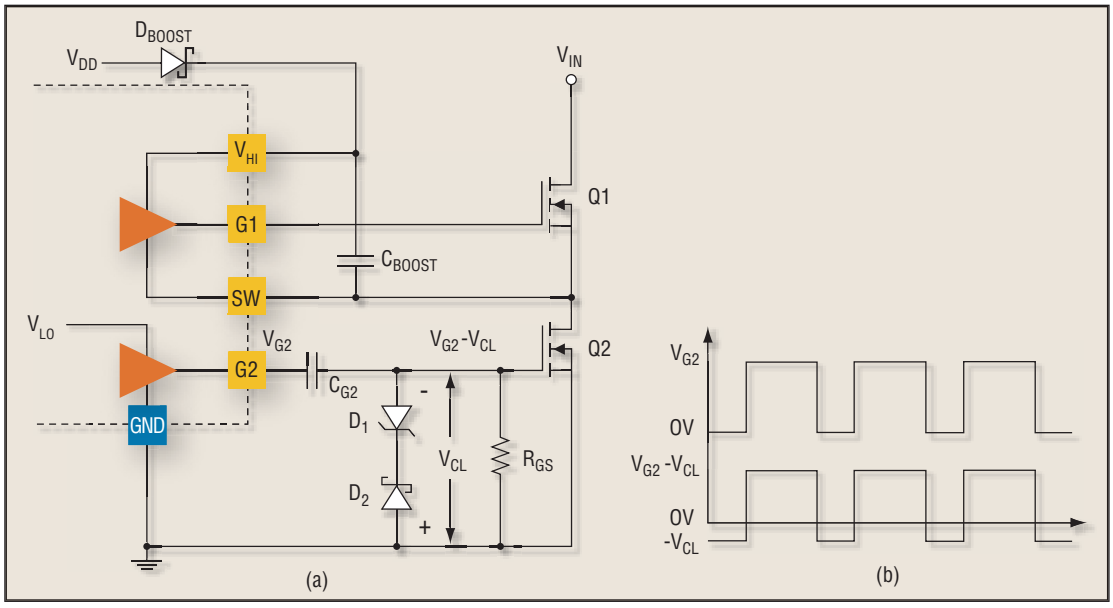

Fig. 7. *An ac-coupled, level-shifted, low-side gate-drive circuit (a) minimizes dv/dt-induced turn-on using the gate-drive waveforms shown here (b).*

Placing a small resistor (R_{HI}) in series with high-side supply voltage can have the same effect without requiring a parallel diode.

The waveforms shown in **Fig. 6** are from a 12-V input, 1.8-V output synchronous buck converter driven by a UCC27223 with an external high-side boost, gate-drive configuration as shown in **Fig. 5**. With R_{HI} = 0 Ω and 15 A of load current, G2 has 2.6 V of dv/dt-induced gate voltage when G1 transitions high. When R_{HI} is changed from 0 Ω to 5.11 Ω, the dv/dt-induced gate voltage on G2 is reduced from 2.6 V to 1.5 V. **Fig. 6** highlights the resultant waveforms for each case to show a direct comparison. The G2 dv/dt effect is reduced by 1.1 V, while the rise time of G1 is slowed down by approximately 10 ns.

Slowing down the rising edge of G1 can provide good results at reducing dv/dt-induced turn-on of the synchronous MOSFET. However, as the high-side gate-drive turn-on is slowed down, the switching losses in Q1 are increased. This may be acceptable as long as the savings in power dissipated due to dv/dt-induced shoot-through current is greater than the power dissipated in Q1 from additional switching losses. The exact point of diminishing return will vary between applications and must be carefully evaluated, especially for high-frequency converters where gate-charge and switching losses can have a compounding effect.

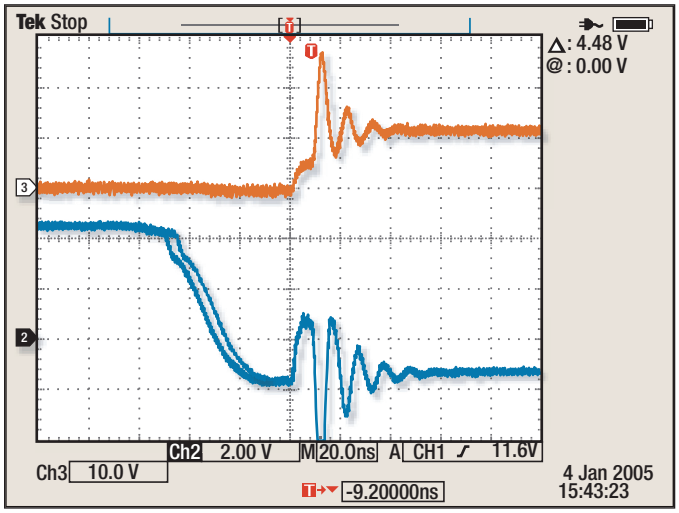

Fig. 8. *The circuit depicted in Fig. 7 configured for a -2-V level shift produces the waveforms shown above.*

For situations in which the additional switching losses taken on by slowing down the rising edge of Q1 are unacceptable, another option may be to level shift the gate drive of G2. In this case, no attempt is made to reduce the dv/dt effect. Rather, by pulling the gate of G2 below ground reference, the dv/dt-induced voltage "bump" still exists but is shifted further below the MOSFET turn-on threshold voltage.

Whereas **Figs. 4** and **5** illustrated circuits to modify the high-side gate drive, the circuit shown in **Fig. 7** minimizes dv/dt-induced turn-on by modifying the low-side gate drive. The timing diagram in **Fig. 7** shows the gate-to-source voltage of Q2 switching between $-V_{CL}$ and $V_{G2} - V_{CL}$. The signal from G2 must first be ac-coupled by properly selecting C_{G2} according to Eq. 6, where Q_{G2} is the total gate charge of Q2, D is the duty cycle, ΔV_{CG2} is the amount of allowable ripple voltage across C_{G2} and F_{SW} is the converter switching frequency:

$$C_{G2} = \frac{Q_{G2}}{\Delta V_{CG2}} + \frac{V_{G2} \times (1-D) \times D}{\Delta V_{CG2} \times R_{GS} \times F_{SW}} \quad \text{(Eq. 6)}$$

The function of R_{GS} is to hold the gate low during initial power-up and to provide a path for current to flow through C_{G2} when V_{G2} is pulled low during the off state of Q2. From the previous example, $V_{G2} = V_{LO} = 6.5$ V, and selecting a 1-kΩ value for R_{GS}, limiting the ripple voltage across C_{G2} to 10%, and using a value of Q_{G2} = 53 nC, C_{G2} is calculated as:

$$C_{G2} = \frac{53\ \text{nC}}{0.1 \times 6.5\ \text{V}} + \frac{6.5\ \text{V} \times (1-0.15) \times 0.15}{(0.1 \times 6.5\ \text{V}) \times 1\ \text{k}\Omega \times 300\ \text{kHz}} = 86\ \text{nF} \approx 100\ \text{nF} \quad \text{(Eq. 7)}$$

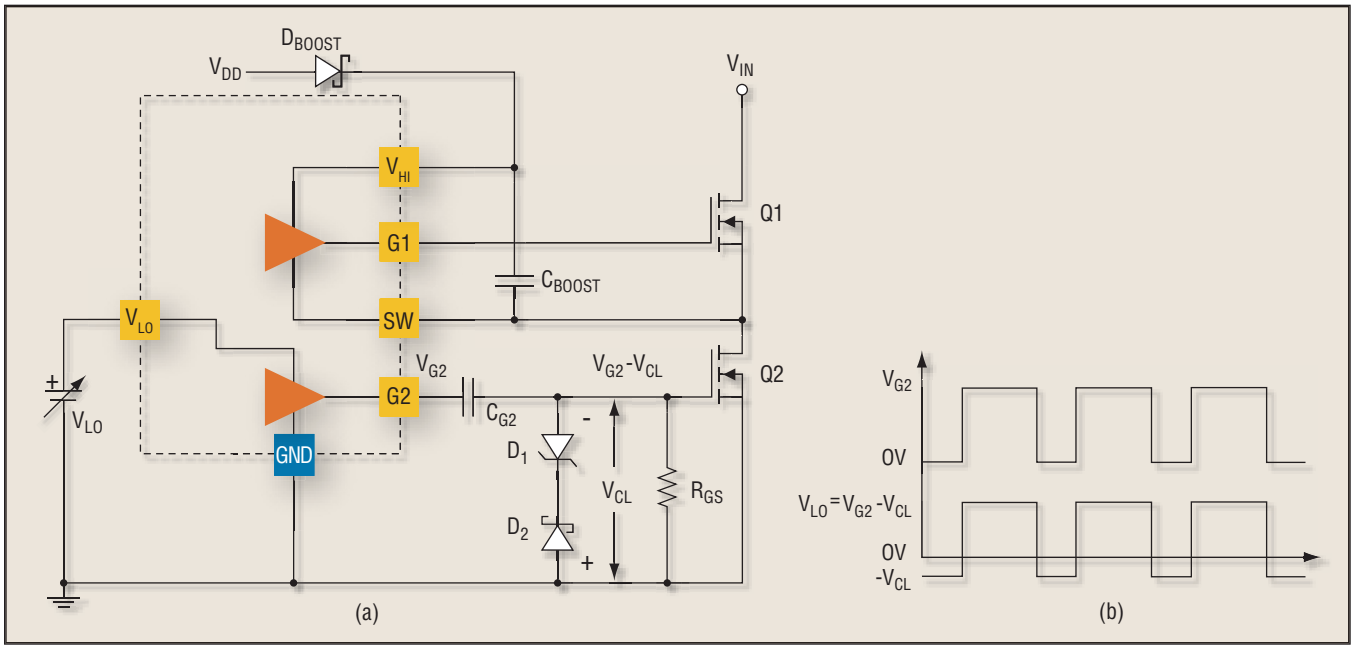

Fig. 9. *Tradeoffs between MOSFET operating characteristics and gate-drive amplitude can be compensated for by using a gate-drive circuit with adjustable amplitude (a) to produce the gate-drive waveforms shown here (b).*

Since the dv/dt-induced voltage on G2 was measured as 2.6 V from **Fig. 6**, a 2.5-V zener diode and a low-voltage BAT54-type Schottky diode can be used for D1 and D2. The clamp voltage (V_{CL}) can be calculated as the difference between the zener voltage (V_Z) of D1 and the forward voltage drop (V_F) of D2:

$$V_{CL} = V_Z - V_F = 2.5\ V - 0.5\ V = 2\ V \qquad \text{(Eq. 8)}$$

The waveforms shown in **Fig. 8** were taken from the

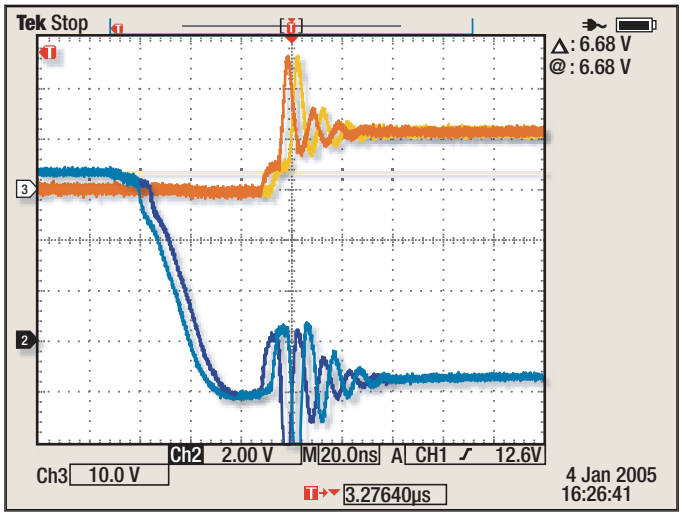

Fig. 10. *An ac-coupled low-side gate driver circuit with a -2-V level shift and adjustable amplitude produces the waveforms shown here.*

circuit shown in **Fig. 7** with component values calculated from Eqs. 7 and 8. The 2.6-V dv/dt-induced voltage is still present on G2, but only reaches a maximum amplitude of approximately 0.6 V. As expected, the maximum V_{GS} amplitude of Q2 has now been reduced to 4.48 V. If a 3-V zener diode were used for D1, the dv/dt voltage spike would be completely level shifted below ground reference but the maximum drive amplitude would only be 4 V.

The design tradeoff for the circuit of **Fig. 7** is that as the V_{GS} drive amplitude of Q2 is reduced, the operating characteristics of Q2 are also affected. For a 12-V to 1.8-V converter, the low-side MOSFET is commutating the full-load current, averaged over 1 D. Therefore, the on-resistance of Q2 must be as low as possible. However, as V_{GS} decreases, $R_{DS(ON)}$ increases. By referring to the manufacturer's $R_{DS(ON)}$ versus V_{GS} curve for a HAT2165 MOSFET, the on-resistance increases by approximately 0.6 mΩ for a 2-V decrease in V_{GS} from 6.5 V to 4.5 V. Similarly, the total gate charge also decreases from 53 nC to 33 nC, but the resulting efficiency contribution from gate-charge savings is minimal when compared to the added conduction loss taken on from the increase in $R_{DS(ON)}$.

This tradeoff between MOSFET operating characteristics and gate-drive amplitude can be compensated for by using a gate-drive circuit with adjustable amplitude.

The circuit in **Fig. 9** offers the ultimate flexibility in terms of dealing with dv/dt-induced turn-on effect. All of the benefits discussed can be applied without incurring any of the drawbacks. The high-side MOSFET is fully switched with no added external resistance, the low-side MOSFET can be fully level shifted to within the $-V_{GS}$ limits of the device and the operating characteristics of the low-side MOSFET can be optimized by selecting the appropriate value for V_{LO}.

The waveforms shown in **Fig. 10** were recorded from a power stage driven by a UCC27223 synchronous buck MOSFET driver that uses a dithering technique known as predictive gate drive. By adjusting the external V_{LO} drive bias to approximately 8.5 V, the amplitude of G2 is corrected to account for the voltage lost due to the level-shifting operation. This technique can offer the greatest benefit to high-frequency, high-current, 12-V synchronous buck applications such as multiphase voltage regulator modules (VRMs).

Key Points for Improving DV/DT Immunity

To summarize, here are five key points listed in order of lowest to highest complexity:

1. Choose a low-side MOSFET with a $Q_{GD}/Q_{GS(TH)}$ ratio that is less than 1.
2. Select a combination MOS/bipolar-MOSFET drive stage with minimum pull-down resistance for the low-side MOSFET.
3. Slow down the turn-on of high-side gate drive (tradeoff: switching loss in high-side MOSFET).
4. AC couple and level shift the low-side drive (tradeoff: conduction loss in low-side MOSFET).
5. AC couple and level shift the low-side drive with adjustable drive amplitude to optimize MOSFET $R_{DS(ON)}$ and gate-charge characteristics.

At the very least, the first and second points should be considered for all synchronous converter applications. For lower-frequency converters, it may be helpful to allow component placeholders in the design schematic to control the rising and falling edges of the high-side gate drive, as highlighted in the third point. Designers should consider the fourth and fifth key points if either they have experienced dv/dt-induced turn-on problems in previous designs or they anticipate possible dv/dt problems due to MOSFETs not selected according to Eq. 5.

In most cases, a power supply designer gives very little forethought to designing a converter that is optimized for dv/dt robustness. And since dv/dt-induced turn-on is a parasitic high-frequency phenomenon, implementing a fix after the fact can be difficult. However, following a few, simple up-front design steps, combined with good layout techniques, can help assure the best possible switching performance from your synchronous buck power stage. **PETech**

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