OV7620 SINGLE-CHIP CMOS VGA COLOR DIGITAL CAMERA
OV7120 SINGLE-CHIP CMOS VGA B&W DIGITAL CAMERA

Description

The OV7620 (color) and OV7120 (black and white) CMOS Image sensors are single-chip video/imaging camera devices designed to provide a high level of functionality in a single, small-footprint package. The devices incorporate a 640 x 480 image array capable of operating at up to 30 frames per second. Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming. All required camera functions including exposure control, gamma, gain, white balance, color matrix, color saturation, hue control, windowing, and more, are programmable through the serial SCCB interface. The device can be programmed to provide image output in different 16-bit and 8-bit formats.

Features

- 326,688 pixels, 1/3" lens, VGA/QVGA format
- Progressive scan/Interlaced scan
- 8-bit/16-bit Data output formats - YCrCb 4:2:2 ITU-656, IR-601 GRB 4:2:2 & RGB Raw Data
- Wide dynamic range, anti-blooming, zero smearing
- Electronic exposure/gain/white balance control
- Image controls - brightness, contrast, gamma, saturation, sharpness, windowing, hue, etc.
- Internal & external synchronization

- Line exposure option
- 5 Volt operation, low power dissipation
  - < 120 mA active power at 30FPS
  - < 10 µA in power-down mode
- Built in Gamma correction (0.45/0.55/1.00)
- SCCB programmable:
  - Color saturation, brightness, hue, white balance, exposure time, gain, etc.

Ordering Information

Product	Package	Description
OV7620	**48 LCC** **0.560 in^2**	**COLOR, VGA, QVGA, Digital, SCCB interface**
OV7120	**48 LCC** **0.560 in^2**	**VGA, QVGA, Digital, SCCB interface**

Applications

. Video Conferencing
. Video Phone
. Video Mail
. Still Image
. PC Multimedia

Key Specifications

Array Element(VGA) **(QVGA)**	640x480 (320x240)
Pixel Size	7.6µm x 7.6µm
Image Area	4.86mm x 3.64mm
Max Frames/Sec	Up to 60 FPS for QVGA
Electronics Exposure	Up to 648:1 (for selected FPS)
Scan Mode	Progressive or Interlace
Gamma Correction	128 Curve Settings
Min. Illumination (3000K)	OV7620 < 2.5 lux @ f1.4 OV7120 < 0.5 lux @ f1.4
S/N Ratio	> 48 dB (AGC off, Gamma=1)
FPN	< 0.03% V_{PP}
Dark Current	< 1.9nA/cm^2
Dynamic Range	> 72 dB
Power Supply	5VDC± 5%
Power Requirements	< 120mA Active < 10µA Standby
Package	48 pin LCC

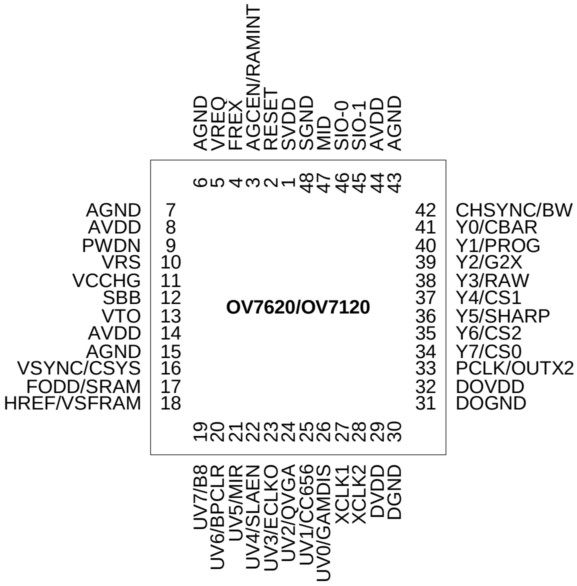

Figure 1. OV7620/OV7120 Pin Diagram

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Pin Description

Table 1. Pin Description

Pin No.	Name	Pin Type	Function/Description
1	SVDD	V_{IN}	Sensing Power (+5V) pins.
8, 14,44	AVDD	V_{IN}	Analog Power (+5V) pins.
29	DVDD	V_{IN}	Digital Power (+5V) pins.
32	DOVDD	V_{IN}	Digital I/O Power (+5V / +3.3V) pins.
48	SGND	V_{IN}	Sensing ground connections. Connect to supply common
6, 7, 15, 43	AGND	V_{IN}	Analog ground connections. Connect to supply common
30	DGND	V_{IN}	Digital ground connection. Connect to supply common
31	DOGND	V_{IN}	Digital Output ground connection.
2	RESET	I	Chip reset, “high” active.
3	AGCEN/RAMINT	I	AGCEN =1 enables the Auto Gain Control. AGCEN = 0 disables it. This pin setting is effective when pin SBB = 1. RAMINT=1 initializes frame transfer.
4	FREX	I	Frame exposure control input, effective in progressive scan only. The positive width of FREX defines the exposure time.
5	VrEQ	V_{REF}	Internal voltage reference. Requires an 0.1uF decoupling capacitor to ground.
9	PWDN	Function (Default=0)	PWDN =1 puts chip in power down (sleep) mode.
10	VrS	V_{REF}	Internal voltage reference. Requires an 0.1uF decoupling capacitor to ground.
11	VcCHG	V_{REF}	Internal voltage reference. Requires an 1.0uF decoupling capacitor to ground.
12	SBB	I	SBB = 1 selects the power-up method of programming the internal functions. SBB = 0 selects the SCCB pin programming method. Results of the power-up method can only be changed by a new power-up or reset sequence.
13	VTO	O	Video Test Output (NTSC)
16	VSYNC/CSYS	O	VSYNC: Vertical sync output. This pin is asserted high during several scan lines in the vertical sync period. CSYS: Composite Sync. When not using SCCB, a 10k pull up changes pin 42(CHSYNC) to CSYS.
17	FODD/SRAM	O	FODD: Odd field flag. Asserted high during the odd field, low during the even field. SRAM: External SRAM
18	HREF/VSFRAM	O	HREF: Horizontal window reference output. HREF is high during the active pixel window, otherwise low. VSFRAM: Vertical Sync Frame.
19	UV7/B8	O	UV7: Digital output UV bus. UV7 used for 16-bit operation for outputting chrominance data. B8: Switch for 8-bit mode luminance/Chroma tristate. Default is 16-bit mode.
20	UV6/BPCLR	O	UV6: Digital output UV bus. UV6 used for 16-bit operation for outputting chrominance data. BPCLR: Bypass RGB color matrix.
21	UV5/MIR	O	UV5: Digital output UV bus. UV5 used for 16-bit operation for outputting chrominance data. MIR: Mirror.
22	UV4/SLAEN	O	UV4: Digital output UV bus. UV4 used for 16-bit operation for outputting chrominance data. SLAEN: Slave Enable.
23	UV3/ECLKO	O	UV3: Digital output UV bus. UV3 used for 16-bit operation for outputting chrominance data. ECKLO: Swap clock output - changes pin 17(FODD) to XCLK out.

Pin No.	Name	Pin Type	Function/Description
24	UV2/QVGA	O	UV2: Digital output UV bus. UV2 used for 16-bit operation for outputting chrominance data. QVGA: QVGA format (320x240)
25	UV1/CC656	O	UV1: Digital output UV bus. UV1 used for 16-bit operation for outputting chrominance data. CC656: CCIR 656 mode.
26	UV0/GAMDIS	O	UV0: Digital output UV bus. UV0 used for 16-bit operation for outputting chrominance data. GAMDIS: Disables Chroma Gamma (RGB).
27, 28	XCLK1, XCLK2	I/O	XCLK1 and XCLK2 are the input/output of the on-chip video oscillator. Nominal crystal clock frequency is 27MHz. If an external clock is used, input to XCLK1, leave XCLK2 unconnected.
33	PCLK/OUTX2	O	PCLK: Pixel clock output. By default, data is updated at the falling edge of PCLK and is stable at its rising edge. PCLK runs at the pixel rate in 16-bit bus operations and twice the pixel rate in 8-bit bus operations OUTX2: Doubles current output.
34	Y7/CSO	O	Y7: Digital output Y bus. In a 16-bit operation, the luminance data is clocked out of this bus at the rate of one byte per pixel. In 8-bit operation, the luminance data and the chrominance data is multiplexed to this bus. CSO: ID configuation bit for the SCCB slave ID.
35	Y6/CS2	O	Y6: Digital output Y bus. In a 16-bit operation, the luminance data is clocked out of this bus at the rate of one byte per pixel. In 8-bit operation, the luminance data and the chrominance data is multiplexed to this bus. CS2: ID configuation bit for the SCCB slave ID.
36	Y5/SHARP	O	Y5: Digital output Y bus. In a 16-bit operation, the luminance data is clocked out of this bus at the rate of one byte per pixel. In 8-bit operation, the luminance data and the chrominance data is multiplexed to this bus. SHARP: Enable Analog Sharpness.
37	Y4/CS1	O	Y4: Digital output Y bus. In a 16-bit operation, the luminance data is clocked out of this bus at the rate of one byte per pixel. In 8-bit operation, the luminance data and the chrominance data is multiplexed to this bus. CS1: ID configuration bit for the SCCB slave ID.
38	Y3/RAW	O	Y3: Digital output Y bus. In a 16-bit operation, the luminance data is clocked out of this bus at the rate of one byte per pixel. In 8-bit operation, the luminance data and the chrominance data is multiplexed to this bus. RAW: Raw Data.
39	Y2/G2X	O	Y2: Digital output Y bus. In a 16-bit operation, the luminance data is clocked out of this bus at the rate of one byte per pixel. In 8-bit operation, the luminance data and the chrominance data is multiplexed to this bus. G2X: Gain 2X.
40	Y1/PROG	O	Y1: Digital output Y bus. In a 16-bit operation, the luminance data is clocked out of this bus at the rate of one byte per pixel. In 8-bit operation, the luminance data and the chrominance data is multiplexed to this bus. PROG: Progressive Scan Mode.
41	Y0/CBAR	O	Y0: Digital output Y bus. In a 16-bit operation, the luminance data is clocked out of this bus at the rate of one byte per pixel. In 8-bit operation, the luminance data and the chrominance data is multiplexed to this bus. CBAR: Color Bar Test Pattern.
42	CHSYNC/BW	O	CHSYNC: Digital output for either composite sync or horizontal sync signal. BW: Enables Black & White.
45	SIO-1	I	SCCB Serial clock input with schmitt trigger.
46	SIO-0	I	SCCB Serial data, input with schmitt trigger.

Pin No.	Name	Pin Type	Function/Description
47	MID	I	Enables multiple SCCB slave IDs. MID = 1 SCCB slave ID is configurable through power-up setting in CS(2:0) MID = 0 SCCB slave ID is preset to 42H/43H.
1	SVDD	V_{IN}	Sensing Power (+5V) pins.
8, 14,44	AVDD	V_{IN}	Analog Power (+5V) pins.
29	DVDD	V_{IN}	Digital Power (+5V) pins.
32	DOVDD	V_{IN}	Digital I/O Power (+5V / +3.3V) pins.
48	SGND	V_{IN}	Sensing ground connections. Connect to supply common

Legend: (I=Input), (O=Output), (I/O=Bi-directional), (P=Power), (A=Analog)

Electrical and Mechanical Characteristics

Table 2. General Characteristics

Descriptions	Min	Max	Units
Operating temperature	0	40	°C
Storage temperature	-40	125	°C
Operating humidity	TBD	TBD	
Storage humidity	TBD	TBD	

Table 3. DC Characteristics (0°C ≤ TA ≤ 85°C, Voltages referenced to GND)

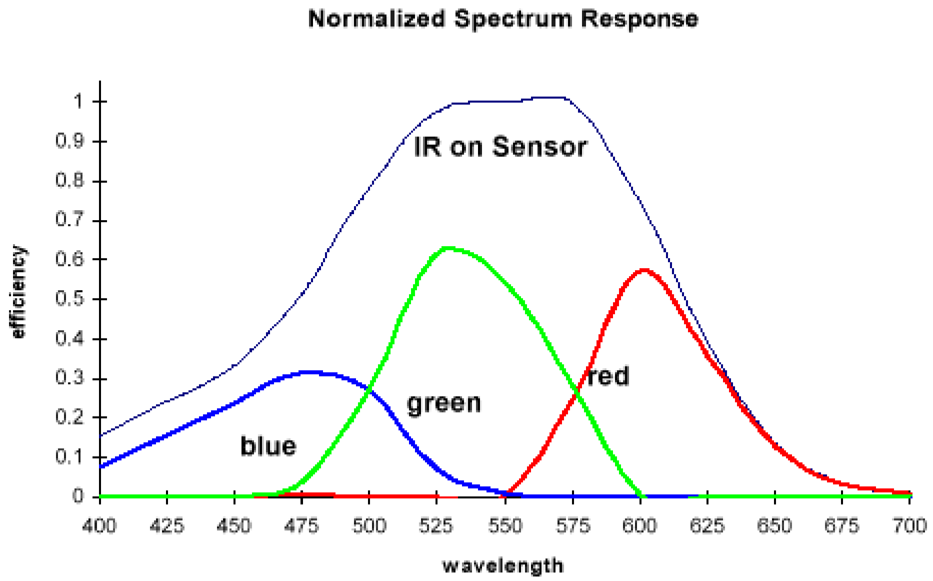
Symbol	Descriptions	Max	Typ	Min	Units
Supply					
V_{DD1}	Supply voltage—internal analog (DEVDD, ADVDD, AVDD, SVDD, DVDD)	5.25	5.0	4.75	V
V_{DD1}	Supply voltage—internal digital & output digital (DOVDD)	5.5 3.6	5.0 3.3	4.5 3.0	V
I_{DD1}	Supply current (V_{DD}=3V, @50Hz frame rate without digital I/O loading.		30		mA
I_{DD2}	Standby supply current	15	5		µA
Digital Inputs					
V_{IL}	Input voltage LOW	0.8			V
V_{IH}	Input voltage HIGH			2	V
C_{IN}	Input capacitor	10			pF
Digital Outputs (standard loading 25pF, 1.2KΩ to 3V)					
V_{OH}	Output voltage HIGH			2.4	V
V_{OL}	Output voltage LOW	0.6			V
SCCB Input					
V_{IL}	SIO-C and SIO-D (V_{DD2}=5V)	1.5	0	-0.5	V
V_{IH}	SIO-C and SIO-D (V_{DD2}=5V)	V_{DD}+0.5	5	3.0	V
V_{IL}	SIO-C and SIO-D (V_{DD2}=3V)	1	0	-0.5	V
V_{IH}	SIO-C and SIO-D (V_{DD2}=3V)	3.5	3	2.5	V

Table 4. AC Characteristics (T_A=25°C, V_{DD}=3V)

Symbol	Descriptions	Max	Typ	Min	Units
RGB/YCrCb Output					
I_{SO}	Maximum sourcing current		15		mA
V_Y	DC level at zero signal Y_{PP} 100% amplitude (without sync) Sync amplitude		1 1 0.3		V
ADC Parameters					
B	Analog bandwidth		TBD		MHz
Φ_{DIFF}					
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		0.5		LSB

Table 5. Timing Characteristics

Symbol	Descriptions	Max	Typ	Min	Units
Oscillator and Clock Input					
f_{OSC}	Frequency (XCLK1)	30	27	10	MHz
t_r, t_f	Clock input rise/fall time	5			ns
	Clock input duty cycle	55	50	45	%
t_{BUF}	Bus free time between STOP and START			1.3	µs
$t_{HD:SAT}$	SIO-D change after START status			0.6	µs
t_{LOW}	SIO-D low period			1.3	µs
t_{HIGH}	SIO-D high period			0.6	µs
$t_{HD:DAT}$	Data hold time			0	µs
$t_{SU:DAT}$	Data setup time			0.1	µs
$t_{SU:STP}$	Setup time for STOP status			0.6	µs
Digital Timing					
t_{PCLK}	PCLK cycle time 16-bit operation 8-bit operation			 74 37	 ns ns
t_r, t_f	PCLK rise/fall time	15			ns
t_{PDD}	PCLK to data valid	15			ns
t_{PHD}	PCLK to HREF delay	20	5	0	ns



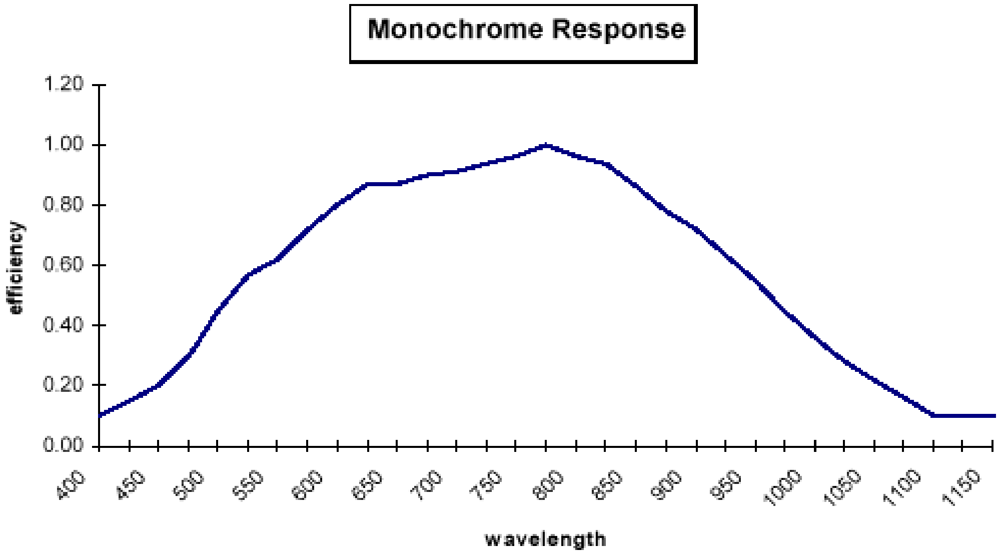


Figure 2. OV7620/7120 Light Response

0.1 OV7620/OV7120 7120CHIP OPERATION

Referring to FIG 0.1, OV7620/OV7120 includes a 664x492 resolution image array, an analog signal processor, dual 10bit A/D converters, analog video mux, digital data formatter and video port, SCCB interface with its registers, the digital controls including timing block, exposure block and white balance.

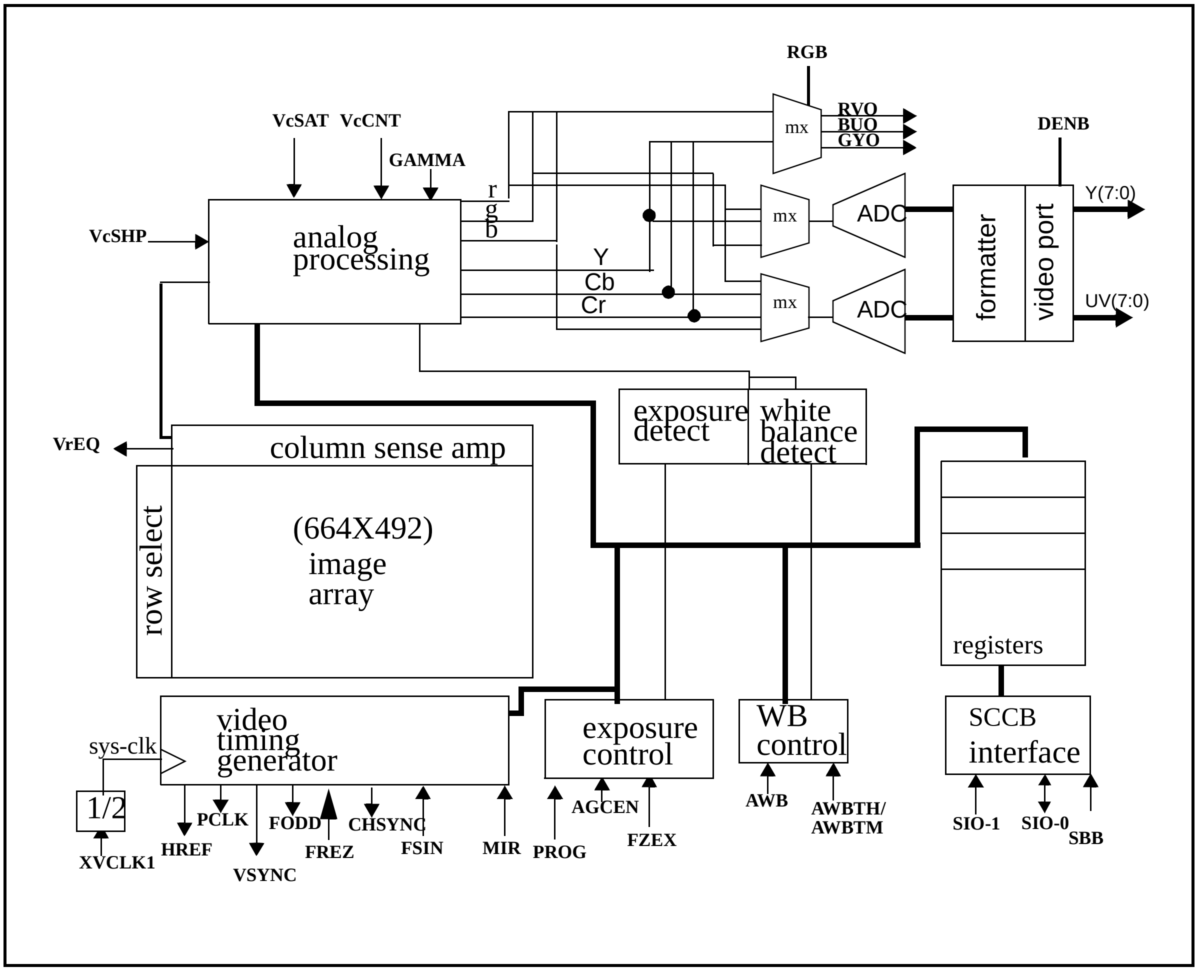


FIG 0.1 OV7620/OV7120 Block Diagram

The OV7620/OV7120 is a 1/3 inch CMOS imaging device. The sensor contains approximately 326,688 pixels. It is base on field integration read-out system with line-by-line transfer and an electronic shutter with synchronous pixel readout scheme. The color filter of the sensor consists of primary color RG/GB array arranged in line-alternating fashion.

The majority of signal processing is performed in the analog processing block, which does color separation, matrixing, AGC, gamma correction, color correction, color balance, black level calibration, knee smooth, aperture correction, controls for the luminance and chrominance picture and anti-alias filtering. The analog video signals are based on the formula:

$Y = 0.59G + 0.31R + 0.11B$; where R,G,B is the equivalent color components in each pixel
$U = R-Y$;
$V = B-Y$;

Another output data format is YCrCb, its formula is as follows:
$Y = 0.59G + 0.31R + 0.11B$
$Cr = 0.713 \times (R - Y)$
$Cb = 0.564 X (B - Y)$

The YCrCb /RGB Raw Data signal is fed to two 10 bit A/D converters, one for the Y/R&G channel, one is shared by Cr&Cb / B&G channels. The A/D converted data stream is further conditioned in the digital formatter, finally the 16bit or 8 bit data muxing is done in the digital video port.

The on-chip 10 bit A/D can operate up to 13.5 MSPS, since it is fully synchronous to the pixel rate, the conversion rate always follows the frame rate. An A/D black-level-calibration circuitry ensures the black level of Y/RGB is translated to value 16, and the peak white level is limited to 240; CrCb black level is 128, Peak/Bottom is 240/16. RGB raw data output range is 16/240, 0 & 255 reserved for sync flag. Also OV7620/OV7120 support non-CCIR standard output range, that is 1/254, 0 and 255 are reserved for sync flag.

The computation in the electronic exposure control is based on the brightness of the full image. The exposure algorithm is optimized for normal scene which assuming the subject is well-lit relative to the background. In case of a different backlight condition, there is also a AEC White/ Black ratio selection register, which can be used as AEC algorithm adjustment to get special image. Along with the AEC is the on chip AGC which can boost gain up to 24dB if needed. To achieve proper color temperature, auto or manual white balance control is also available. There is a separate saturation, brightness contrast and sharpness adjustment for further fine tuning of the picture quality. OV7620/OV7120 provide a set of register to control White Balance ratio register which can be used as increase/decrease image field Red/Blue component ratio. In most case, the default setting may be sufficient.

The windowing feature allows the user to size the window according to their need. The window is sizable from 4X2 to 664x492 and can be placed anywhere inside the 664X492 boundary. Noted this function does not change the frame rate or data rate, it simply change the assertion of the **HREF** to match with the horizontal and vertical region that is programmed by the user. A typical application for this is hardware zooming, and panning. Default output window is 640x480.

The digital video port offers 16 bit 4:2:2 format complying to the 60Hz **CCIR601** timing standard. OV7620/OV7120 also supports 8 bit data format in Cb Y Cr Y order by using port Y only and running at twice the pixel rate while the port UV is inactive. Other than the 16 bit data bus, OV7620/OV7120 supplies standard video timing signals such as **VSYNC**, **HREF**, **PCLK**, **FODD, CHSYNC.**

OV7620/OV7120 support standard **ZV** Port Interface Timing. It provides **VSYNC**, **CHSYNC**, **PCLK** and 16 Bit data bus: **Y<7:0>** and **UV<7:0>**. **PCLK** rising edge clock data bus into **ZV** port.

To decrease data transfer rate while high resolution image unnecessary, OV7620/OV7120 provides a solution, that is it can output **QVGA** resolution image. This mode decrease pixel rate one half. The resolution default value is 320x240 and can be programmable. Every line only output one half data. For Interlaced Mode, all field line output (320), for Progressive Scan Mode, only one half line data output.

The digital video port also offer **RGB Raw Data** 16 Bit/8 Bit format. The output sequence is matched to OV7620/OV7120 Color Filter Pattern, that is UV channel output sequence is G R G R ..., Y Channel output sequence is B G B G,....To 8 Bit RGB Raw data output format, just use Y channel and disable UV channel, output sequence is B G R G ....

OV7620/OV7120 supports **CCIR656** YCrCb 4:2:2 digital output format. The **SAV**(Start of Active Video) and **EAV**(End of Active Video) is just at the beginning and the end of **HREF** window. So the position of **SAV** and **EAV** is changing with active pixel window. Also you can get 8 bit **RGB raw data** with **SAV** and **EAV** information.

OV7620/OV7120 support some flexible YUV output format. One is standard YUV 4:2:2. Another is U V sequence swap format, that means UV channel output V U V U ...(16 Bit) and V Y U Y ...(8 Bit). The 3rd format is Y/UV sequence swap in 8 Bit output, that is Y U Y V ....

OV7620/OV7120 can be use as **black**&**white** camera. At this mode, it's vertical resolution will be higher than color mode. All data will be output from Y port and UV port will be tri-state. Data (Y/RGB) output rate is same as 16 Bit mode.

OV7620/OV7120 can be programmable to swap Y/UV or RGB output byte MSB and LSB. Y7 - Y0 default sequence is Y7 is MSB and Y0 is LSB. When swap, Y7 is LSB and Y0 is MSB, relative middle bits are swapped.

An important factor about digital camera is how convenient the interface is, OV7620/OV7120 has made the frame rate programmable and the A/D synchronous to the actual pixel rate. Essentially, it is a whole image capture system in a single chip. Since the internal AEC has a range of 1:260, and AGC have 24dB, for the most of applications, the camera can adjust itself to meet the lighting condition without user intervention.

OV7620/OV7120 support hardware/software RESET function: when **RESET** pin tie to high, whole chip will be reset including all register. Hardware sleeping mode: when **PWDN** tie to high, chip clock will be stop and internal circuit reset except all SCCB register. Also there is a SCCB control software reset control register 12 bit 7, which is same as hardware **RESET** pin function.

OV7620/OV7120 hardware reset time minimum is 1 ms.

OV7620/OV7120 support hardware/software power saving mode. When the **PWDN** pin tie to high, whole chip will be set to power down status without any current consumption. For software power down control, all current set to zero except crystal circuit. In power down mode, all SCCB register value will be kept.

Two control mechanism have been built into OV7620/OV7120: **A**. one time read-in of pin states at **power up** or **RESET** status, including hardware and software reset; **B**. SCCB interface. Two methods are mutually exclusive, only one is used at a time, selected by pin **SBB**. Method A has limited access to full chip features.

The power up reset method is a one time setting, the setting can not be altered later. The pins used in the control are shared with the digital video port data bus. At power up, the video port is initially tri-stated, allowing the external pull-up/pull-down resistor to set the default operating conditions, 2048 clocks later the video port resumes normal function. The detail of the power up pin control method is explained in the individual pin out section.

SCCB interface provides full access to all the features. The detail is in the SCCB register set.

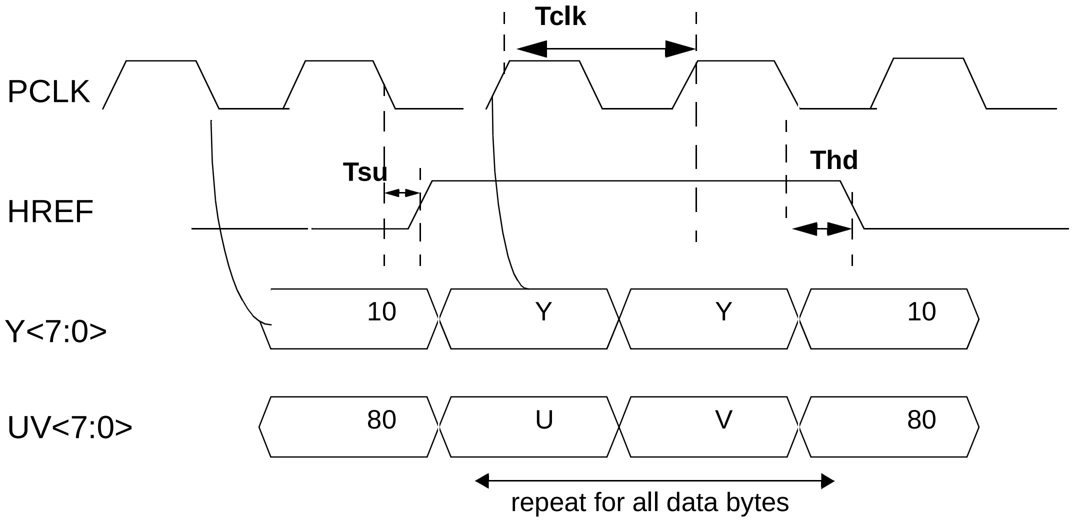
0.2 VIDEO FORMAT

Table 1.1: 4:2:2 16 bit Format

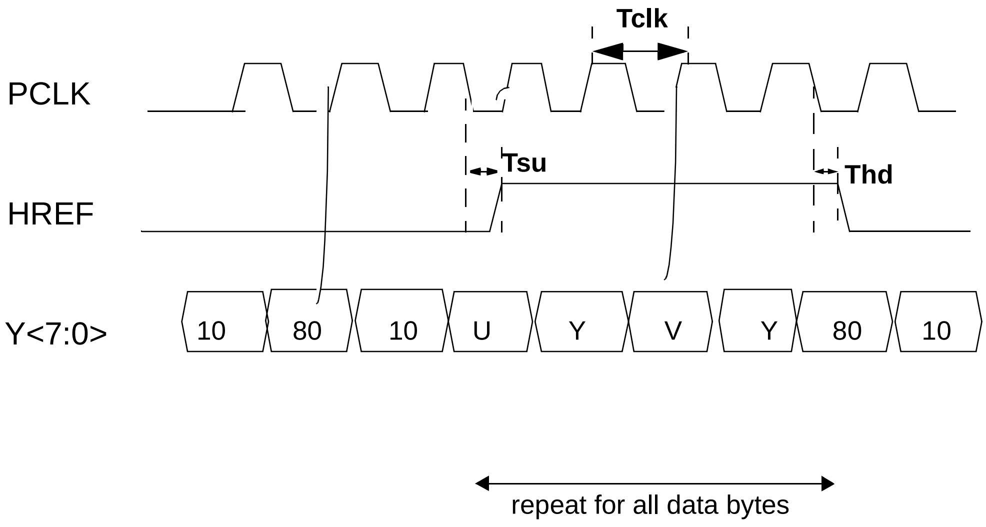
Data Bus	**Pixel Byte Sequence**					
Y7	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0	Y0	Y0	Y0	Y0	Y0	Y0
UV7	U7	V7	U7	V7	U7	V7
UV6	U6	V6	U6	V6	U6	V6
UV5	U5	V5	U5	V5	U5	V5
UV4	U4	V4	U4	V4	U4	V4
UV3	U3	V3	U3	V3	U3	V3
UV2	U2	V2	U2	V2	U2	V2
UV1	U1	V1	U1	V1	U1	V1
UV0	U0	V0	U0	V0	U0	V0
Y FRAME	0	1	2	3	4	5
UV FRAME	0		2		4	

Table 1.2: 4:2:2 8 bit Format

Data Bus	**Pixel Byte Sequence**							
Y7	U7	Y7	V7	Y7	U7	Y7	V7	Y7
Y6	U6	Y6	V6	Y6	U6	Y6	V6	Y6
Y5	U5	Y5	V5	Y5	U5	Y5	V5	Y5
Y4	U4	Y4	V4	Y4	U4	Y4	V4	Y4
Y3	U3	Y3	V3	Y3	U3	Y3	V3	Y3
Y2	U2	Y2	V2	Y2	U2	Y2	V2	Y2
Y1	U1	Y1	V1	Y1	U1	Y1	V1	Y1
Y0	U0	Y0	V0	Y0	U0	Y0	V0	Y0
Y FRAME	0		1		2		3	
UV FRAME	0 1				2 3			



Pixel Data 16 bit Timing
Use PCLK rising edge latch data bus



Pixel Data 8 bit Timing
Use PCLK rising edge latch data bus

FIG 0.2 Pixel Data Bus (YUV Output)

Note: **Tclk** is pixel clock period. When OV7620/OV7120 system clock is 27MHz, Tclk=74ns for 16 Bit output; Tclk=37ns for 8 Bit output. **Tsu** is HREF set-up time, maximum is 15 ns; Thd is HREF hold time, maximum is 15 ns.

0.3 RGB Raw Data Format

RGB Raw data output from Y and UV port.

UV port output data sequence: G R G R G R ... or B R B R ...(refer to register 28 bit 2)

Y port output data sequence: B G B G B G ... or G G G G ...(refer to register 28 bit 2)

Array Color Filter Patter is Bayer-Pattern

Table 1.3:

R\C	1	2	3	4	.	641	642	643	644
1	B_{11}	G_{12}	B_{13}	G_{14}		B	G	B	G
2	G_{21}	R_{22}	G_{23}	R_{24}		G	R	G	R
3	B_{31}	G_{32}	B_{33}	G_{34}		B	G	B	G
4	G_{41}	R_{42}	G_{43}	R_{44}		G	R	G	R
5	B_{51}	G_{52}	B_{53}	G_{54}		B	G	B	G
.									
481	B	G	B	G		B	G	B	G
482	G	R	G	R		G	R	G	R
483	B	G	B	G		B	G	B	G
484	G	R	G	R		G	R	G	R
485	B	G	B	G		B	G	B	G

0.3.1 Interlaced Mode 16 Bit Format (HREF total 242)

0.3.1.1 Default mode: In **ODD FIELD**, 1st HREF output UV channel is 2nd line: G_{21} R_{22} G_{23} R_{24}... and Y channel is Row 1: B_{11} G_{12} B_{13} G_{14} ... . 2nd HREF output UV channel output 4th line: G_{41} R_{42} G_{43} R_{44} ... and Y port output 3rd line: B_{31} G_{32} B_{33} G_{34} ... , so on. Data bus should be latched by PCLK rising edge and related to the exact physical position **In Even FIELD,** 1st HREF Y channel output B_{31} G_{32} B_{33} G_{34} ... and UV channel output G_{21} R_{22} G_{23} R_{24} ...2nd HREF Y channel output B_{51} G_{52} B_{53} G_{54} ... and UV output G_{41} R_{42} G_{43} R_{44} ....

0.3.1.2 YG mode: In **ODD FIELD,** 1st HREF Y channel output G_{21} G_{12} G_{23} G_{14} ... and UV channel is B_{11} R_{22} B_{13} R_{24} .... 2nd HREF Y channel output G_{41} G_{32} G_{43} G_{34} ... and UV channel output B_{31} R_{42} B_{33} R_{44} .... In **EVEN FIELD**, 1st HREF Y channel output G_{21} G_{32} G_{23} G_{34} ... and UV channel output B_{31} R_{22} B_{33} R_{24} ... 2nd HREF channel output G_{41} G_{52} G_{43} G_{54} ... and UV channel output B_{51} R_{42} B_{53} R_{44} ...

0.3.2 Progressive Scan Mode 16 Bit Format (HREF total 484)

0.3.2.3 Default mode: 1st HREF UV channel output unstable data, Y output B_{11} G_{12} B_{13} G_{14} .... 2nd HREF UV channel output G_{21} R_{22} G_{23} R_{24} ..., Y output B_{11} G_{12} B_{13} G_{14} ... 3rd HREF UV channel output G_{21} R_{22} G_{23} R_{24} ..., Y output B_{31} G_{23} B_{33} G_{34} .... Every line data output twice.

0.3.2.4 YG mode: 1st HREF Y and UV output unstable data. 2nd HREF Y channel output G_{21} G_{12} G_{23} G_{14} ..., UV output B_{11} R_{22} B_{13} R_{24} ... 3rd HREF Y is G_{21} G_{32} G_{23} G_{34} ..., UV channel is B_{31} R_{22} B_{33} R_{24} ... Every line data output twice.

0.3.2.5 One line mode: 1st HREF Y channel output B_{11} G_{12} B_{13} G_{14} ..., 2nd HREF Y channel output G_{21} R_{22} G_{23} R_{24} ..., so on. UV channel tri-state.

0.3.3 Interlaced Mode 8 Bit (242 HREF)

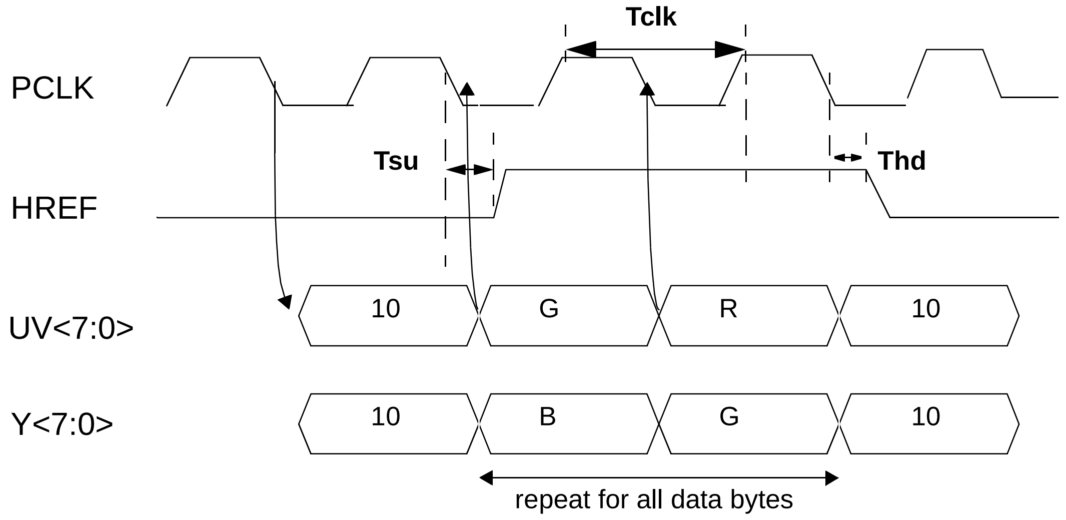
0.3.3.6 ODD FIELD: 1st HREF Y channel output B11 G21 R22 G12 ... 2nd HREF Y channel output B31 G41 R42 G32..., so on. PCLK timing is double and use PCLK rising edge latch data bus. UV channel tri-state**.**

0.3.3.7 EVEN FIELD: 1st HREF Y channel output B31 G21 R22 G32 ... 2nd HREF Y channel output B51 G41 R42 G52 ..., so on. PCLK timing is double and data bus should be latched by its rising edge. UV channel tri-state**.**

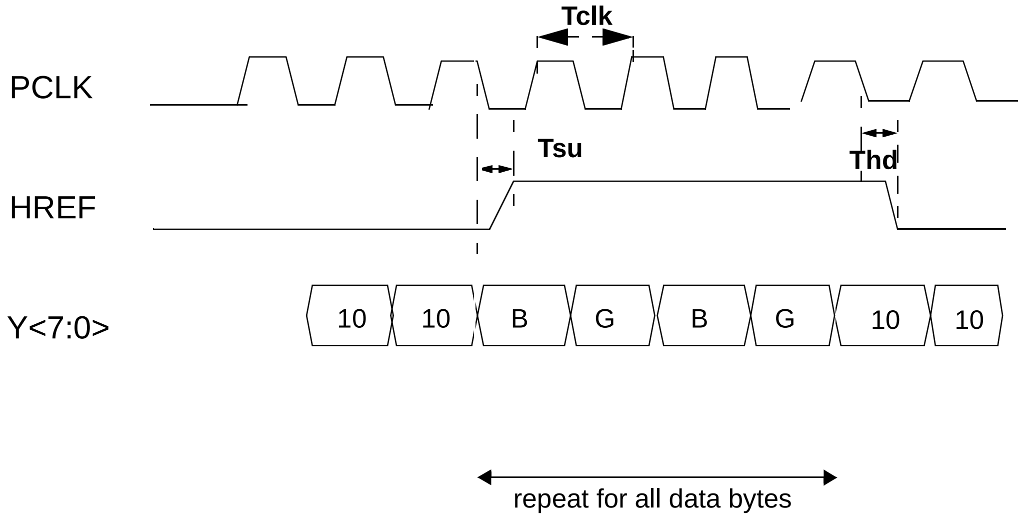
0.3.4 Progressive Scan Mode 8 Bit (484 HREF)

0.3.4.8 1st HREF Y channel output unstable data. 2nd HREF Y channel output B11 G21 R22 G12 ... 2nd HREF Y channel output B31 G21 R22 G32 ..., so on. PCLK timing is double and PCLK rising edge latch data bus. UV channel tri-state. Every line data output twice**.**

RGB raw data timing chart is as follows:



Pixel Data 16 bit Timing
PCLK rising edge latch data bus



Pixel Data 8 bit Timing
PCLK rising edge latch data bus

FIG 0.3 Pixel Data Bus (RGB Output)

Note: **Tclk** is pixel clock period. When OV7620/OV7120 system clock is 27MHz, Tclk=74ns for 16 Bit output; Tclk=37ns for 8 Bit output. **Tsu** is HREF set-up time, maximum is 15 ns; **Thd** is HREF hold time, maximum is 15 ns.

0.4 ZV Port Interlace Timing

The ZV Port is a single-source uni-directional video bus between a PC Card socket and a VGA controller. The ZV Port complies with CCIR601 timing to allow NTSC decoders to deliver real-time digital video straight into the VGA frame buffer from a PC Card. OV7620/OV7120 support ZV Port Timing, which output signal can be output to a PC Card directly, then to VGA controller. The timing is as below:

FIG 0.4 ZV Port Timing

Notes: ZV Port format output signal include:

- **VSYNC**: Vertical sync pulse.
- **HREF**: Horizontal valid data output window.
- **PCLK**: Pixel clock used to clock valid data and CHSYNC into ZV Port. Default frequency is 13.5MHz when use 27MHz as system clock. Rising edge of PCLK is used to clock the 16 Bit data.
- **Y<7:0>**: 8 Bit luminance data bus..
- **UV<7:0>**: 8 Bit chrominance data bus.

All Timing Parameters is list in following table.‘

Table 1.4: ZV Port AC Parameter

Symbol	Parameter	Min.	Max.
t1	PCLK fall timing	4 ns	8 ns
t2	PCLK low time	30 ns	
t3	PCLK rise time	4 ns	8 ns
t4	PCLK high time	30 ns	
t5	PCLK period	74 ns	
t6	Y/UV/HREF setup time	10 ns	
t7	Y/UV/HREF hold time	20 ns	
t8	VSYNC setup/hold time to HREF	1 us	

Note: In Interlaced Mode, there are Even/Odd field different (t8). When In Progressive Scan Mode, only frame timing same as Even field(t8).

After **VSYNC** falling edge, OV7620/OV7120 will output black reference level, the line number is **Tvs**, which is the line number between the 1st **HREF** rising edge after **VSYNC** falling edge and 1st valid data **CHSYNC** rising edge. Then valid data, then black reference, line number is **Tve**, which is the line number between last valid data **CHSYNC** rising edge and 1st **CHSYNC** rising edge after **VSYNC** rising edge. The black reference output line number is dependent on vertical window setting.

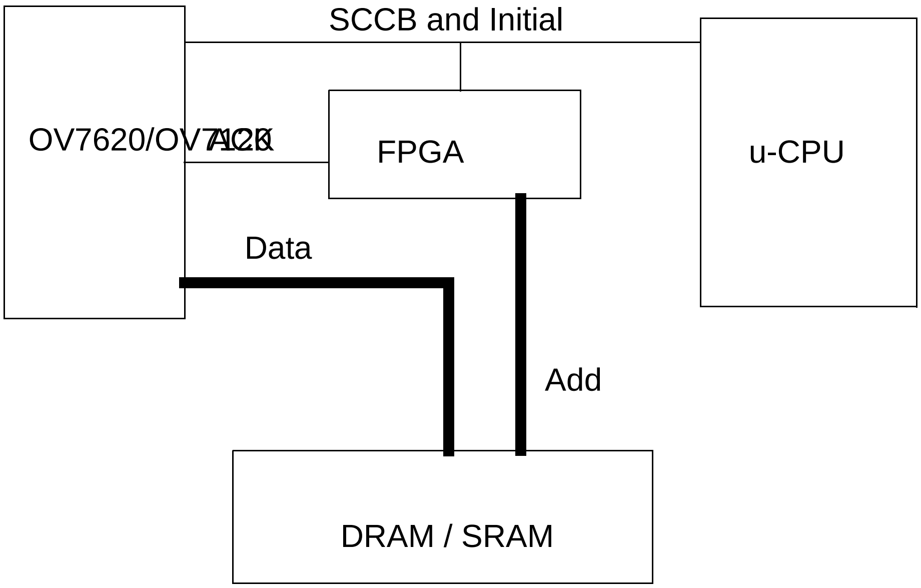
When in default setting, **Tvs** = 14***Tline**, which is changed with register register 19<7:0>. If in **Interlaced Mode**, register 19<7:0> change 1 step, **Tvs** increase 1 line. If in **Progressive Scan Mode**, register 19<7:0> step equal to 2 line.

When in default setting, **Tve** = 4***Tline** for **Odd** Field, **Tve** = 3***Tline** for **Even** Field, which is changed with register register 1A<7:0>. If in **Interlaced Mode**, register 1A<7:0> change 1 step, **Tve** increase 1 line. If in **Progressive Scan Mode**, register 1A<7:0> step equal to 2 line.

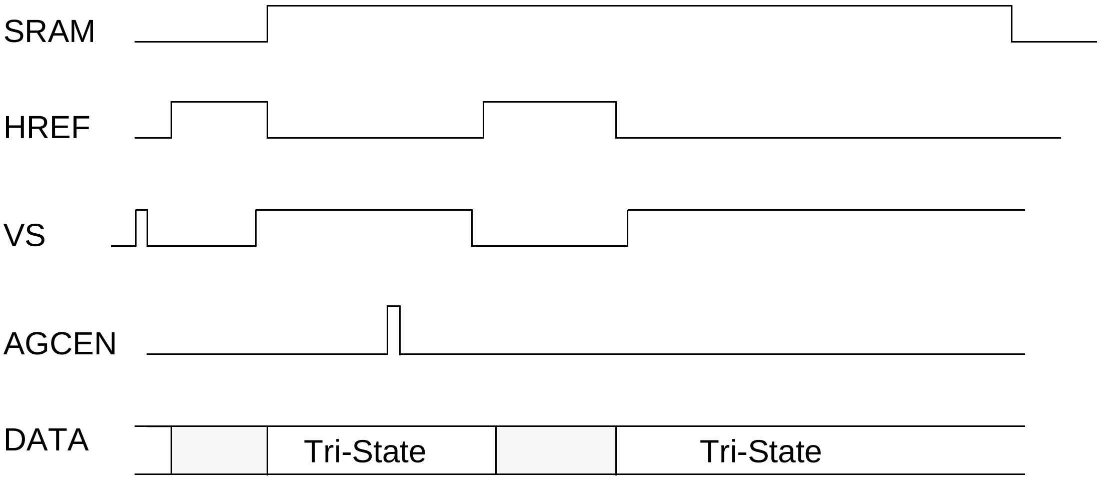
In **Progressive Scan Mode**, **Tve** = 3***Tline** and **Tvs** = 35***Tline**.

0.5 Interface for External RAM Controller and Micro-controller

OV7620/OV7120 can be programmed to output single frame data to external RAM. The structure block diagram is as follows:



The timing diagram is as follows:



SRAM is internal control bit which is high means the OV7620/OV7120 enter external RAM status. This is programmed by SCCB (register **27**) or power-on read-in. When **SRAM**=1, OV7620/OV7120 all data bus will be tri-stated and ready to send the data. Micro-controller will send a initial signal to FPGA to reset all RAM Address block, after that, there are two method to get one frame data frame OV7620/OV7120:

1. Micro-controller send a initial pulse to OV7620/OV7120 **AGCEN** input pin
2. Micro-controller send a SCCB command to program OV7620/OV7120 send Single frame data

The OV7620/OV7120 output signal **VS** is the ACK signal from sensor, when **VS** is high means OV7620/OV7120 is in ready status, when **VS** is low, means OV7620/OV7120 will send one frame data.

0.6 Digital Output Format Table

Table 1.5: Digital Output Format Type

		Interlaced		Progressive Scan	
Resolution		640x480	320x240	640x480	320x240
YUV 4:2:2	16Bit	Y	Y	Y	Y
	8Bit	Y	Y	Y	Y
	CCIR656	Y	Y	Y	Y
RGB	16Bit	Y	Y	Y	Y
	8Bit	Y	Y	Y	Y
	CCIR656[1]	Y	Y	Y	Y
Y/UV swap[2]	16Bit	-	-	-	-
	8Bit	Y	Y	Y	Y
U/V swap	YUV[3]	Y	Y	Y	Y
	RGB[4]	Y	Y	Y	Y
YG	16Bit	Y	Y	Y	Y
	8Bit	-	-	-	-
One Line	16Bit	-	-	Y	-
	8Bit	-	-	-	-
MSB/LSB swap[5]		Y	Y	Y	Y

Note: “Y” in the table means this combination is supported by OV7620/OV7120.

1. RGB CCIR656 format means 4-byte SAV and EAV is inserted at the beginning and ending of HREF, which are used to grab Vsync and Hsync information. So only use 8-bit data bus line and don’t need **VSYNC** and **CHSYNC** signal line.

2. Y/UV swap is valid only in 8 bit output. Y channel output sequence is Y U Y V ... rather U Y V Y ....

3. To YUV format, U/V swap means UV channel output sequence swap. V U V U ... rather U V U V ... for 16 bit; V Y U Y ... rather U Y V Y ... for 8-bit.

4. To RGB format, U/V swap means neighbor row B R output sequence swap. So refer to preview RGB raw data output format, different format change accordingly.

5. MSB/LSB swap means: Default Y/UV channel output port relationship is:

Table 1.6: Default Output Sequence

	MSB							LSB
Output Port	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Internal Output data	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

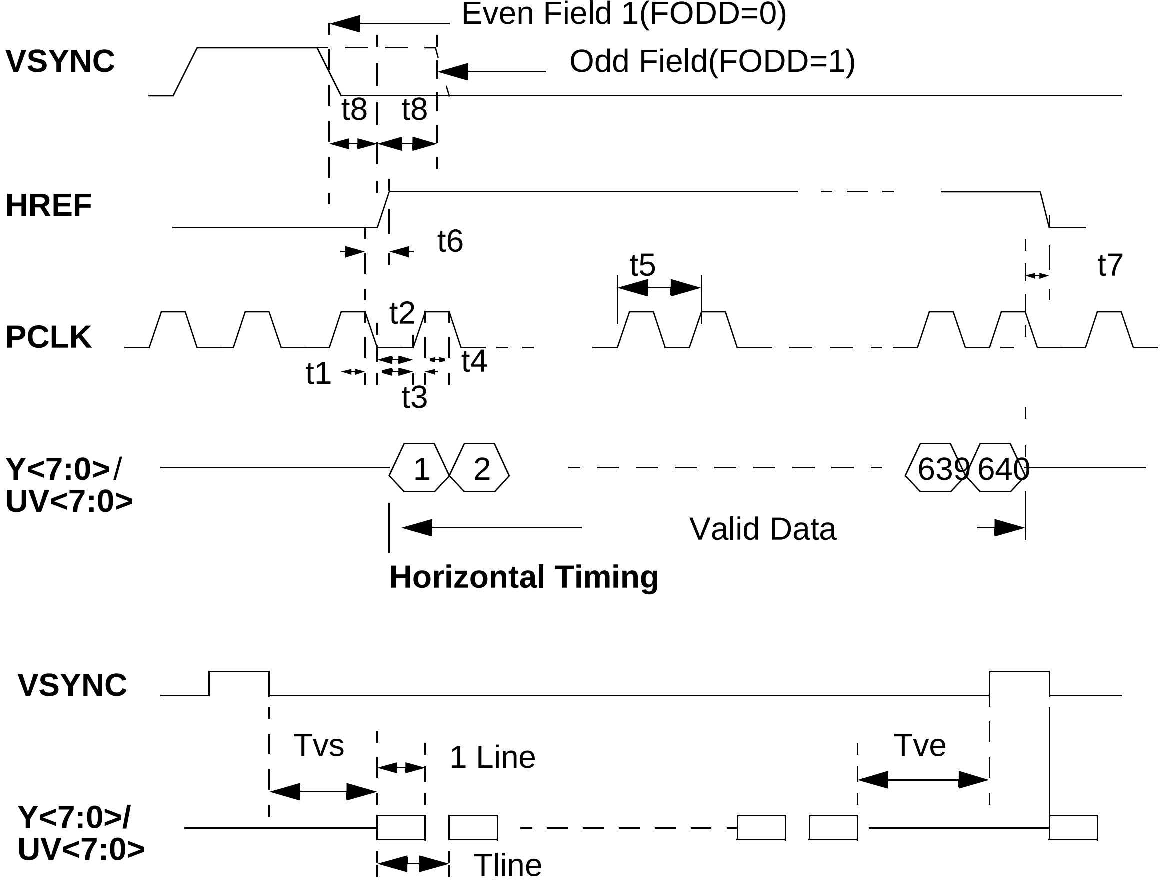
If

6.

7.

8.

9.



0.7 QVGA Resolution Digital Output Format

Table 1.8: QVGA Digital Output Format(YUV, beginning of line)

Pixel #	1	2	3	4	5	6	7	8
Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
UV	U0,V0	U1,V1	U2,V2	U3,V3	U4,V4	U5,V5	U6,V6	U7,V7

0.7.5 Interlaced Mode:

Y channel output Y2 Y3 Y6 Y7 Y10 Y11 ... UV channel output U2 V3 U6 V7 U10 V11 ... Every line output data number is half(320 pixels) and all line data(240 line) in one field will be output.

0.7.6 Progressive Scan Mode:

Y channel output Y2 Y3 Y6 Y7 Y10 Y11 ... UV channel output U2 V3 U6 V7 U10 V11 ... Every line output data number is half(320 pixels) and only one half line data (every other line, total 240 line) in one frame will be output.

0.7.7 QVGA 60 Frame/s Mode:

In Interlace Mode, QVGA mode output frame rate is 30 Frame/s and 60 Field/s. When in 60 Frame/s mode, only Odd field data output and frame rate is 60 Frame/s.

Table 1.9: QVGA Digital Output Format (RGB Raw data, beginning of line)

Pixel #	1	2	3	4	5	6	7	8
Line 1	B0	G1	B2	G3	B4	G5	B6	G7
Line 2	G0	R1	G2	R3	G4	R5	G6	R7

0.7.8 Interlaced Mode (Default RGB two line output mode):

UV channel output G0 R1 G4 R5 G8 R9 ... Y channel output B0 G1 B4 G5 B8 G9 ...Every line output half data(320 pixels) and all line data(240 line) in one field will be output.

0.7.9 Interlaced Mode (YG two line output mode):

Y channel output G0 G1 G4 G5 G8 G9 ... UV channel output B0 R1 B4 R5 B8 R9 ... Every line output half data(320 pixels) and all line data(240 line) in one field will be output.

0.7.10 Progressive Scan Mode (Default RGB two line output mode):

UV channel output G0 R1 G4 R5 G8 R9 ... Y channel output B0 G1 B4 G5 B8 G9 ...Every line output half data(320 pixels) and all line(480 line) data in one frame will be output.

0.7.11 Progressive Scan Mode (YG two line output mode):

UV channel output G0 R1 G4 R5 G8 R9 ... Y channel output B0 G1 B4 G5 B8 G9 ...Every line output half data(320 pixels) and all line(480 line) data in one frame will be output.

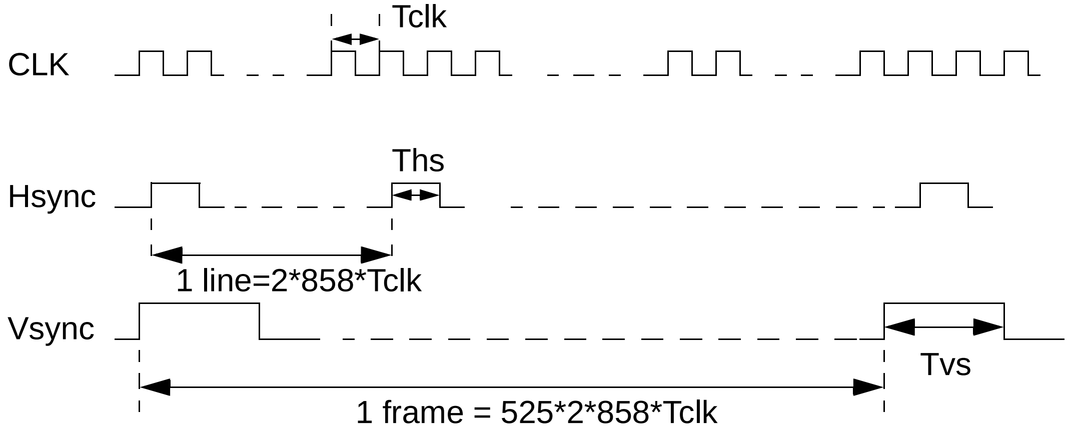
0.8 Slave Mode Operation

OV7620/OV7120 can be programmable to be slave device. Default OV7620/OV7120 is a master device, it provide Hsync, Vsync output. If used as slave device, (register 29 bit 6=1), external master device must provide:

System clock CLK to **XCLK1** pin;
Horizontal sync Hsync to **CHSYNC** pin, positive acted.
Vertical frame sync Vsync to **VSYNC** pin, positive acted.

When in slave mode, OV7620/OV7120 tri-state **CHSYNC** and **VSYNC** output pin and use as input pin. To synchronize the chip, OV7620/OV7120 use external system clock CLK synchronize external horizontal sync Hsync, then use synchronized horizontal sync to synchronize external vertical frame sync Vsync. But to match internal counter, these three must keep exact relation as below:

Hsync period is 2*858 * CLK
Vsync period is 525* 2*858 * CLK



Note: (1) Ths > 6*Tclk (2) Ths < Tvs < 2*858*Tclk

FIG 0.5 Slave Mode External Sync Timing

OV7620/OV7120 will be stable after 1 frame. (2nd Vsync).

0.9 Frame Exposure Mode

OV7620/OV7120 support frame exposure mode when in Progressive Scan Mode. When the **FREX** pin is used as an external master device sets the exposure time. When **FREX** =1, the whole array is precharged. The exposure time is then determined by the external master device which controls **FREX**. When **FREX**=0, the OV7620/OV7120 begins to output data line by line. While data is output, the OV7620/OV7120 must be blocked from light by using a mechanical shutter, so that the whole array is exposed at the same time and has the same exposure period. In default line exposure mode, the array precharge and read mode is first charge 1st line, after one line read out, precharge 2nd line, so on. the width of **FREX**=1 must large the a fixed timing to make sure whole array has been precharged.

Frame exposure mode timing is as below:

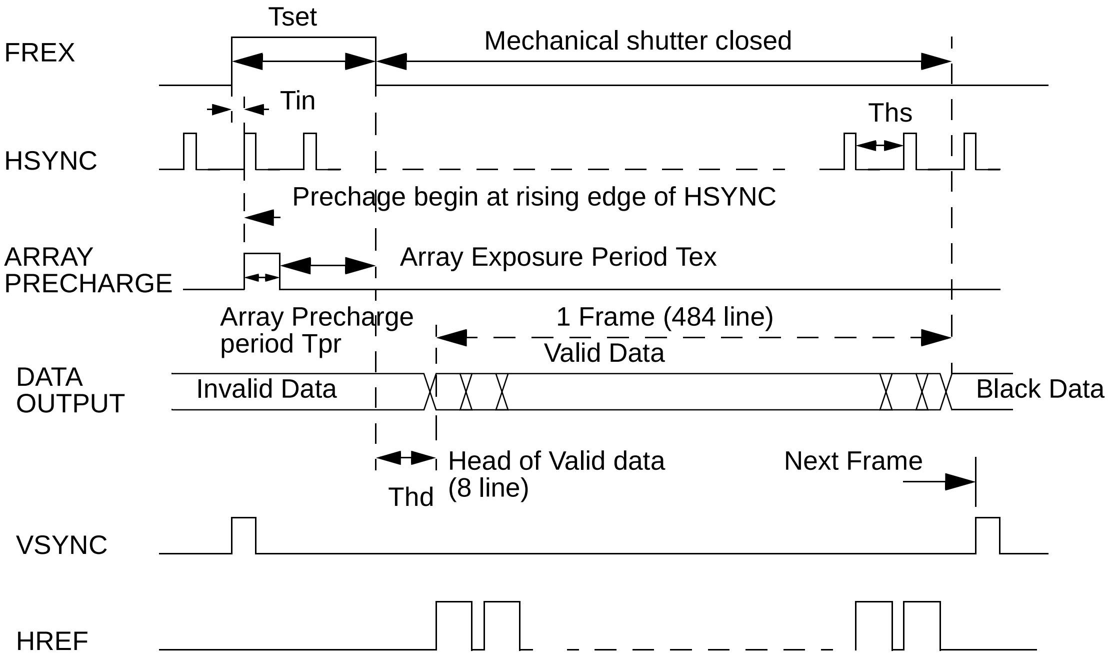

FREX
Tset
Mechanical shutter closed
Tin
Ths
HSYNC
Prechage begin at rising edge of HSYNC
ARRAY PRECHARGE
Array Exposure Period Tex
Array Precharge period Tpr
1 Frame (484 line)
Valid Data
DATA OUTPUT
Invalid Data
Black Data
Head of Valid data (8 line)
Thd
Next Frame
VSYNC
HREF

FIG 0.6 Frame Exposure Timing

Note: Tpr = 492 * 4 * Pclk, Pclk is internal pixel clock. For default 27MHz, Tclk=74 ns. If CLK<5:0> set to divided number, Tclk will increase accordingly.

Tex is array exposure time which is decided by external master device.

Tin is undetermined due to the use of **HSYNC** rising edge to synchronize **FREX**, Tin < Ths

When **FREX**=0, there are 8 lines of data output before valid data output. Thd = 4 * Ths. Valid data is output when **HREF**=1.

Tset = Tin + Tpr + Tex. Tset > Tpr + Tin. Because Tin is uncertain, so exposure time setting resolution is Ths (one line).

0.10 SCCB BUS

SCCB access is enabled only if pin **SBB**=0. OV7620/OV7120 is a slave device that supports 400kbit/s 7bit address data transfer protocol. Within each byte, MSB is always transferred first, read/write control bit is the LSB of the first byte

The protocol requires **SIO-0** must be stable during the HIGH period of the **SIO-1**. Each data bit can only change state when is **SIO-1** LOW.

OV7620/OV7120 reserves **CS(2:0)** for the slave ID, which makes eight slave camera combinations.

OV7620/OV7120 SCCB supports multi-byte write and multi-byte read. In a write cycle, the master must supply the subaddress, however, the master does not supply the subaddress in the read cycle, therefore, OV7620/OV7120 takes the read subaddress from the previous write cycle. In multi-byte write or multi-byte read cycles, the subaddress is auto increment after the first data byte so that continuous locations can be accessed in one bus cycle. Since a multi-byte cycle overwrites its original subaddress, if a read cycle follows immediately to a multi-byte cycle, it is necessary to insert a single byte write cycle that provides a new subaddress.

If OV7620/OV7120 support 400 kBit/s fast SCCB mode, system clock (CLK) must be at least 10 Mhz.

0.11 SCCB REGISTER SETS

OV7620/OV7120 can be configured, by setting pin CS<2:0> high or low at reset/power up, to one of eight slave IDs as listed below, the ID can not be altered once the chip is out of reset or power up state.

Table 1.10: Slave ID

CS<2:0>	000	001	010	011	100	101	110	111
WRITE ID (hex)	42	46	4a	4e	52	56	5a	5e
READ ID (hex)	43	47	4b	4f	53	57	5b	5f

OV7620/OV7120 support two option: **single** chip and **multiple** chip decided by PIN **MID**. If **MID** set to **LOW** (Default value), chip slave ID is **42**(for write) and **43**(for read). If **MID** set to **HIGH**, OV7620/OV7120 can support 8 slave ID selection. Default **MID** is **LOW** by internal setting.

In write cycle, the second byte in SCCB bus is the subaddress for selecting the individual on chip registers, the third byte is the data associated with this register. Writing to unimplemented subaddress and reserved subaddress is ignored.

In read cycle, the second byte is the data associated with the previous stored subaddress. reading of unimplemented subaddress returns unknown.

Registers [00] ~ [02] contains image effect parameters that also can be modified by internal controls in auto adjust mode. This provides a simple way to read out those parameters computed by chip internal controls. To do this, first set the chip in auto adjust mode (Register 13 bit 0=1, register 12 bit 2 = 1, register 12 bit 5=1), wait for the image is stable, the register [00],[01] and [02] will be updated by internal control circuit. Then returns it to manual adjust mode(register 13 bit 0=0), all the registers retain the last adjusted values and can be read or overwritten by external host. When the chip is operated in auto adjust mode(register 13 bit 0=1), register [00] ~ [02] will be update by internal algorithm and if write data to them, there will be no effect on chip parameters. The register data can be read out.

The detailed definitions of each register are described below.

Register 00 - rw: AGC gain control

Bits	Null	AGC6	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0
Default	-	-	0	0	0	0	0	0

AGC<5:0> - gain setting for the entire image channel.
The formula is:
Gain = (AGC<3:0>/16+1)*(AGC<4>+1)*(AGC<5>+1); range (1x ~ 7.75x), AGC<5> and AGC<4> control SA2.

Register 01 - rw: Blue gain control

Bits	BLU7	BLU6	BLU5	BLU4	BLU3	BLU2	BLU1	BLU0
Default	1	0	0	0	0	0	0	0

BLU<6:0> - white balance value for the blue channel.
The formula is:
Blue_gain=1+(BLU<7:0> - [80])/[100]; range (0.5x ~ 1.5x).
BLU<7> - Sign bit. If “1”, Blue gain increase; “0” gain decrease.

Register 02 - rw: Red gain control

Bits	RED7	RED6	RED5	RED4	RED3	RED2	RED1	RED0
Default	1	0	0	0	0	0	0	0

RED<6:0> - white balance value for the red channel.
The formula is:
Red_gain=1+(RED<7:0> - [80])/[100]; range (0.5x ~ 1.5x).
RED<7> - Sign bit. If “1”, Red channel gain increase; “0” gain decrease.

Register 03 - rw: Saturation control

Bits	SAT7	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
Default	1	0	-0	0	0	0	0	0

SAT<7:0> - saturation adjustment for the UV channel based on the default setting;
range (-4dB ~ +6dB). If SAT<7:0> > [80], increase; if SAT<7:0> < [80], decrease.

Register 04 & 05 - w: Reserved Register

This register is reserved for internal test use. Write data to this register will be no function.

Register 06 - rw: Brightness control

Bits	BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0
Default	1	0	0	0	0	0	0	0

BRT<7:0> - brightness adjustment for the Y/RGB channel based on the default setting;
range (-200mv ~ +200mv). If BRT<7:0> > [80], brightness increase; If BRT<7:0> < [80], brightness decrease. This register is auto/manual controllable. If register 2D bit 4=1, this register is controlled by chip automatically, if write value to this register, this value will be updated by internal circuit. Only when register 2D bit 4=0, this register can be set to any value

Register 07 - rw: Angalog Sharpness control

Bits	SHP7	SHP6	SHP5	SHP4	SHP3	SHP2	SHP1	SHP0
Default	1	1	0	0	0	0	1	1

SHP<7:4> - Sharpness Threshold.
SHP<3:0> - Sharpness Magnitude.

Register [08] ~ [0B] - w: Reserved.

These four registers are reserved for internal use. Write data to these registers will not function.

Register 0C - rw: White Balance background control -- Blue channel

Bits	Null	Null	ABLU5	ABLU4	ABLU3	ABLU2	ABLU1	ABLU0
Default	-	-	1	0	0	0	0	0

Changes AWB Hue Control
ABLU<4:0> - White Balance background blue color component ratio adjustment. Adjust resolution is 0.625% and total range is (+20% - -20%) This register is used to offset image background blue component ratio.
ABLU<5> - Sign bit. If “1”, decrease background blue component ratio; “0” increase blue component ratio.

Register 0D - rw: White Balance background control -- Red channel

Bits	Null	Null	ARED5	ARED4	ARED3	ARED2	ARED1	ARED0
Default	-	-	1	0	0	0	0	0

Changes AWB Hue Control
ARED<4:0> - White Balance background red color component ratio adjustment. Adjust resolution is 1.5% and total range is (+20% - -20%) This register is used to offset image background red component ratio.
ARED<5> - Sign bit. If “1”, decrease background red component ratio; “0” increase red component ratio.

Register 0E ~ 0F- rw: Reserved

These two registers are reserved for internal use. Write data to these registers will not function.

Register 10 - rw: Auto-Exposure-Control Register

Bits	AEC7	AEC6	AEC5	AEC4	AEC3	AEC2	AEC1	AEC0
Interlace	0	1	1	1	1	1	1	1
Progressive Scan	1	1	1	1	1	1	1	1

AEC<7:0> - exposure time setting; the formula is
Interlaced: $T_{EXPOSURE} = T_{LINE}$ x AEC(7:0);
Progressive: $T_{EXPOSURE} = T_{LINE}$ x AEC(7:0)x2;
where T_{LINE} = Frame Time / 525
if use 27MHz, T_{LINE} = 63.5 uS
Range is: [00] - [7F] for Interlaced; [00] - [FF] for Progressive Scan.

* This register setting is only effective when operated in manual adjust mode (register 13 bit 0=0). Nevertheless, this register is always accessible through the SCCB bus. If register 13 bit 0=1, this register will be updated by internal circuit according AEC algorithm, and if write special value to this register will be useless. The register value can be read out at any time and latest AEC value will be return. If register 13 bit 0=0, or register 29 bit 7=1, the register will hold last value unchanged (either input from SCCB or AEC algorithm result).

* It generally takes no more than two fields for the image to reach the intended exposure after changing the setting.

Register 11 - rw: Clock rate control

Bits	SYN7	SYN6	CLK5	CLK4	CLK3	CLK2	CLK1	CLK0
Default	0	0	0	0	0	0	0	0

CLK<5:0> - system clock prescaler; this register defines the chip pixel clock rate, clock rate is defined by following fulmar:
(16 Bit mode) PCLK = (CLK_input / ((CLK<5:0> + 1) * 2))
(8 Bit mode) PCLK = (CLK_input / (CLK<5:0> + 1))
SYN<7:6> - Three sync output polarity selection:
SYN7 = 0, SYN6 = 0: HSYNC negative, CHSYNC negative, VSYNC positive edge;
SYN7 = 0, SYN6 = 1:.HSYNC negative, CHSYNC negative, VSYNC negative;
SYN7 = 1, SYN6 = 0: HSYNC positive, CHSYNC negative, VSYNC positive.
SYN7 = 1, SYN6 = 1: HSYNC negative, CHSYNC positive, VSYNC positive.

* The effect of the change is immediate, however, it generally takes about two fields for the image to reach the stable state

.

Register 12 - rw: Common control A

Bits	COMA7	COMA6	COMA5	COMA4	COMA3	COMA2	COMA1	COMA0
Default	0	0	1	0	0	1	0	0

COMA7 - “1” initiates the chip soft reset, the reset takes place after the acknowledge bit is issued, the effect is the same as power up the chip, the chip is initialized to a default state, all registers including SCCB’s contents are set to default, this bit is self cleared after the reset.
COMA6 - “1” selects mirror image
COMA5 - “1” enables AGC. “0” - stop AGC and set register [00] to default value. Only effective in auto adjust mode.
COMA4 - “1” select 8 Bit Digital output format is Y U Y V Y U Y V ...
COMA3 - “1” selects raw data signal as video data output, “0” selects YCrCb as video data output. The selection applies to both analog video and digital video.
COMA2 - “1” enable auto white balance, “0” AWB stop and AWB register [01] and [02] value is held at last updated value. Can used as one-shot AWB mode. Valid only in auto mode.
COMA1 - “1” selects Color Bar Test pattern output.
COMA0 - “1” select precise A/D Black Level Compensation (BLC) line method. “0” use standard black level compensation to do A/D BLC field method which is more stable but less precise.

Register 13 - rw: Common control B

Bits	COMB7	COMB6	COMB5	COMB4	COMB3	COMB2	COMB1	COMB0
Default	-	-	0	0	0	0	0	1

COMB7 - Reserved.
COMB6 - Reserved.
COMB5 - “1” selects 8 bit data format, Y/CrCb and RGB video data is multiplexed to the eight bit **Y** bus, tri-state **UV** bus; “0” selects 16 bit format, data go to both **Y<7:0>** bus and **UV<7:0>** bus.
COMB4 - “0” enables digital output in CCIR601 format. “1” enables CCIR656 format.
COMB3 - “0” selects horizontal sync for output to pin **CHSYNC**, “1” selects composite sync for output.
COMB2 - “1” tri-states bus **Y<7:0>** and **UV<7:0>**, “0” enables both buses.
COMB1 - “1” initiates the single frame transfer, for this function to work, field drop mode (FD<1:0> in register [16]) must set to “OFF”. See figure below. After this bit is set, for Interlaced mode, **HREF** is only asserted for consecutive two fields beginning at Odd field. This bit is cleared automatically at the end of this frame. For Progressive Scan mode, **HREF** is only asserted for one frame. Clearing this bit in the middle of active frame has no effect to the assertion of current **HREF**.
COMB0 - “1” enables auto adjust mode, in this mode, internal exposure circuitry overwrites those parameters in registers [00]~[02], the chip adjusts the image based on a preset algorithm. “0” manual adjust mode.

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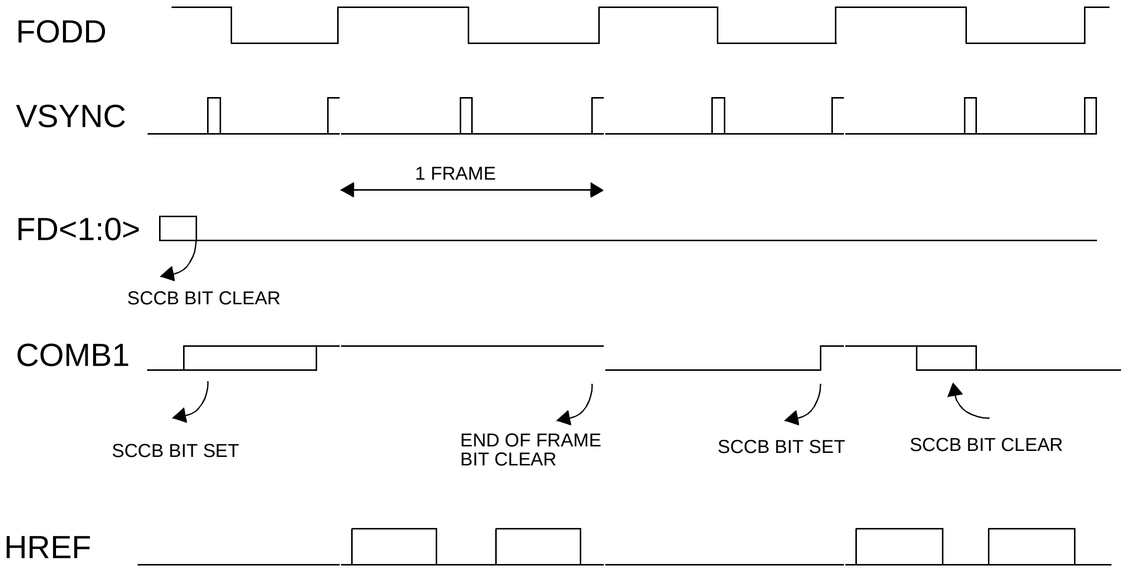


FIG 0.7 Single Frame Transfer Example (Interlaced Mode)

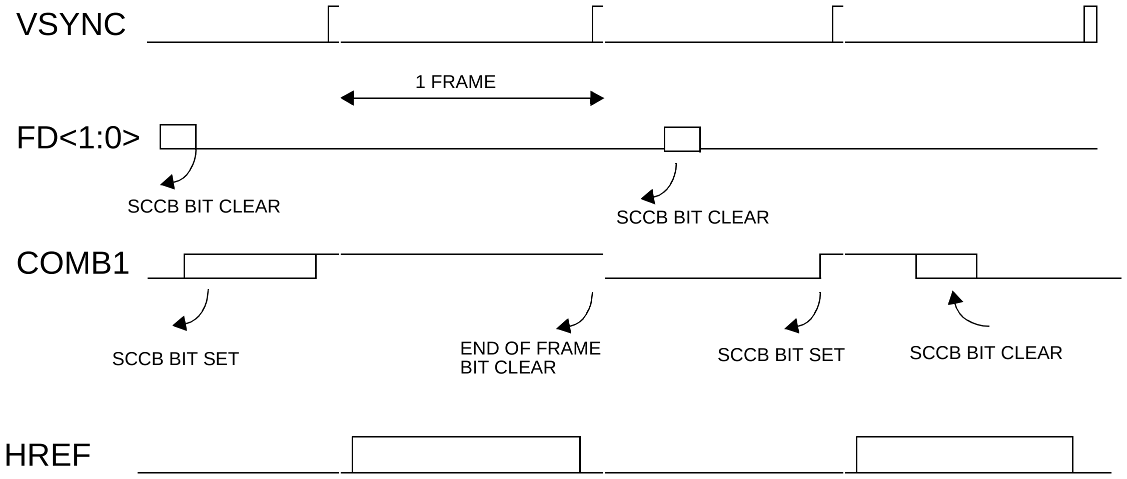


FIG 0.8 Single Frame Transfer Example (Progressive Scan Mode)

Register 14- rw: Common control C

Bits	COMC7	COMC6	COMC5	COMC4	COMC3	COMC2	COMC1	COMC0
Default	0	-	0	0	0	1	-	-

COMC7 - AWB activation threshold selection: 1- high; 0-low.
COMC6 - Reserved.
COMC5 - QVGA digital output format selection. 1 - 320x240; 0 - 640x480.
COMC4 - Field/Frame vertical sync output in VSYNC port selection: 1 - frame sync, only inserted in ODD field vertical sync; 0 - field vertical sync, effect in Interlaced mode
COMC3 - HREF polarity selection: 0 - HREF positive effective, 1 - HREF negative.
COMC2 - RGB gamma selection: 1 - Gamma on, value defined by register [62] value; 0 - gamma is 1 (linear).
COMC1 - Reserved.
COMC0 - Reserved.

Register 15- rw: Common control D

Bits	COMD7	COMD6	COMD5	COMD4	COMD3	COMD2	COMD1	COMD0
Default	-	0	-	-	-	-	-	1

COMD7 - Reserved.
COMD6 - PCLK polarity selection. “0” OV7620/OV7120 output data at PCLK falling edge and data bus will be stable at PCLK rising edge; “1” rising edge output data and stable at PCLK falling edge. When OV7620/OV7120 work as CCIR656 format, COMB4=1, this bit is disable and should use PCLK rising edge latch data bus.
COMD<5:1> - Reserved.
COMD0 - U V digital output sequence exchange control. 0 - V U V U ... for 16Bit, V Y U Y ... for 8 Bit; 1- U V U V ... for 16Bit and U Y V Y ... for 8 Bit.

Register 16 - rw: Frame Drop

Bits	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Default	0	0	0	0	0	0	1	1

FD<7:2>- Frame drop selection, it operates in ODD and EVEN mode as defined by FD<1:0>, it is ignored in OFF & FRAME mode. Its purpose is to divide the video signal into programmed number of time slots in unit of field/frame, and to allow HREF to be active only one field/frame during the period. This function does not affect the video data or pixel rate.

000000 - 000001: disable digital data output, only output black reference level.
000010 - 111111: Output 1 of (2 ~ 63) frame. If set register 33 bit 1= 1, that means only drop 1 frame from (2 ~ 63) frame.

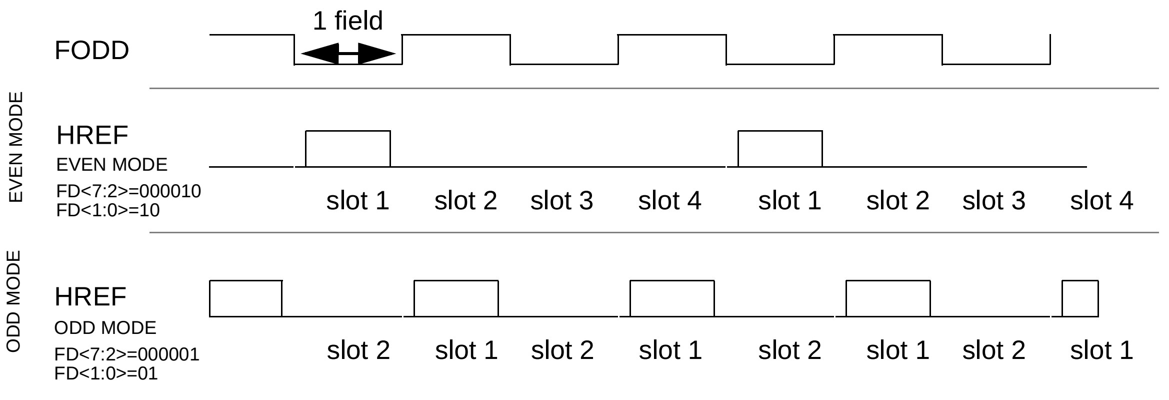


FIG 0.9 Field Division Examples (Interlaced Mode)

Interlaced:
FD<1:0>- field mode selection. Each frame consists of two fields: Odd & Even, these bits defines the assertion of HREF in relation to the two fields.

- 00 - OFF mode; HREF is not asserted in both fields, one exception is the single frame transfer operation (see the description for the register [13])
- 01 - ODD mode; HREF is asserted in odd field only.
- 10 - EVEN mode; HREF is asserted in even field only.
- 11 - FRAME mode; HREF is asserted in both odd field and even field. FD<7:2> useless (default).

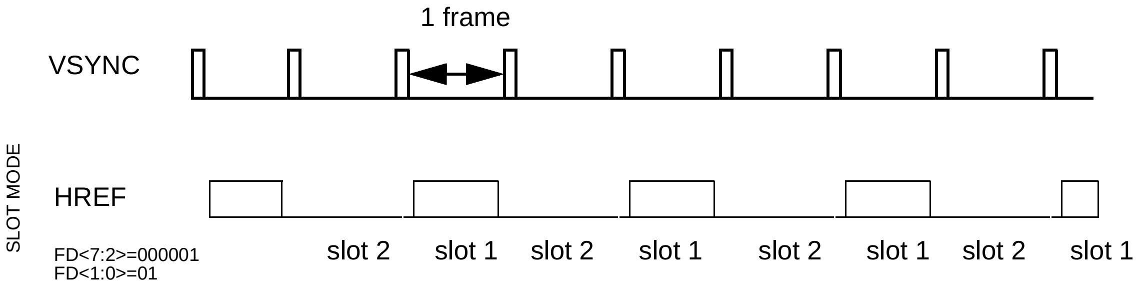


FIG 0.10 Frame Division Examples (Progressive Scan Mode)

Progressive Scan:
FD<1:0> - frame mode selection.

- 00 - OFF mode; HREF is not asserted in both fields, one exception is the single frame transfer operation (see the description for the register [13])
- 01,10 - SLOT mode; HREF is asserted in frame according FD<7:2>.
- 11 - FRAME mode; HREF is asserted in every frame. FD<7:2> useless

Register 17 - rw: Horizontal Window start

Bits	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0
Default	0	0	1	0	1	1	1	1

HS<7:0> - selects the starting point of HREF window, each LSB represents four pixels for Interlaced/Progressive full resolution mode, two pixels for QVGA resolution mode, this value is set based on an internal column counter, the default value corresponds to 640 horizontal window. Maximum window size is 664. see window description below. HS<7:0> programmable range is [2C]- [D2], and should less than HE<7:0>. HS<7:0> should be programmable to value larger than or equal to [2C]. Value larger than [D2] is invalid. See Figure 1.14.

Register 18 - rw: Horizontal Window end

Bits	HE7	HE6	HE5	HE4	HE3	HE2	HE1	HE0
Default	1	1	0	0	1	1	1	1

HE<7:0> - selects the ending point of HREF window, each LSB represents four pixels for full resolution and two pixels for QVGA resolution, this value is set based on an internal column counter, the default value corresponds to the last available pixel. The HE<7:0> programmable range is [2D] - [D2]. HE<7:0> should be larger than HS<7:0> and less than or equal to [D2]. Value larger than [D2] is invalid. See Figure 1.14.

Register 19- rw: Vertical Window start

Bits	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0
Default	0	0	0	0	0	1	1	0

VS<7:0> - selects the starting row of vertical window, in full resolution mode, each LSB represents 1scan line in one field for Interlaced Mode, 2 scan line in one frame for Progressive Scan Mode. In QVGA resolution (set by register 14 bit 5), each LSB represents 1 scan line in one field for Interlaced Mode, 1scan line in one frame for Progressive Scan Mode. See Figure 1.14. Min. is [05], max. is [F6] and should less than VE<7:0>.

Register 1A- rw: Vertical Window end

Bits	VE7	VE6	VE5	VE4	VE3	VE2	VE1	VE0
Default	1	1	1	1	0	1	0	1

VE<7:0>- selects the ending row of vertical window, in full resolution mode, each LSB represents 1scan line in one field for Interlaced Mode, 2 scan line in one frame for Progressive Scan Mode. In QVGA resolution, each LSB represents 1 scan line in one field for Interlaced Mode, 1scan line in one frame for Progressive Scan Mode. See Figure 1.14. Min. is [05], max. is [F6] and should larger than VS<7:0>.

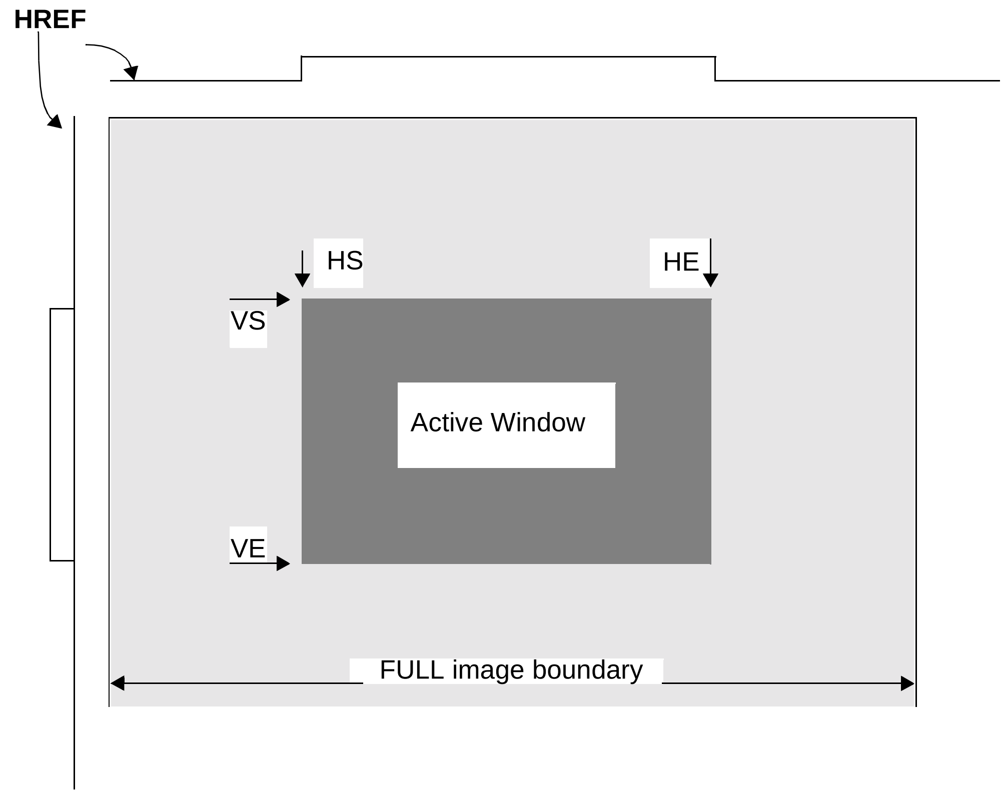


FIG 0.11 Window Sizing

As shown above, HS<7:0> defines the starting pixel within a scan line, HE<7:0> defines the ending pixel within a scan line. VS<7:0> defines the starting row within a field, VE<7:0> defines the ending row within a field. VS/VE automatically defines the window height of a image frame. The rectangular window defined by HS/HE/VS/VE is the active image window. Only pixels insides this window is valid, along with the **HREF** timing signals, black level substitutes the pixel data when outside the active window.

Identical value for HS/HE or VS/VE is not permitted since it causes undefined window size.

If end point is lower than the starting point, the window begins from the starting point and ends at the far end of the available image boundary.

The window size calculate formula is as below:

1. Horizontal size: VGA mode: Horizontal window size = (Register [18] - Register [17])*4.
   QVGA mode: Horizontal window size = (Register [18] - Register [17])*2.
2. Vertical size: VGA mode: Vertical window size = (Register [1A]- Register [19]+1);
   QVGA mode: Horizontal window size = (Register [1A] - Register [19]+ 1).

Register 1B- rw: Pixel shift

Bits	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0
Default	0	0	0	0	0	0	0	0

PS<7:0> - to provide a way to fine tune the output timing of the pixel data relative to that of **HREF**, it physically shifts the video data output time early or late in unit of pixel clock as shown in the figure below. This function is different from changing the size of the window as is defined by HS<7:0> & HE<7:0> in register [17] and [18].

The number of pixels that can only be shifted late. Maximum shift pixel number is 255.

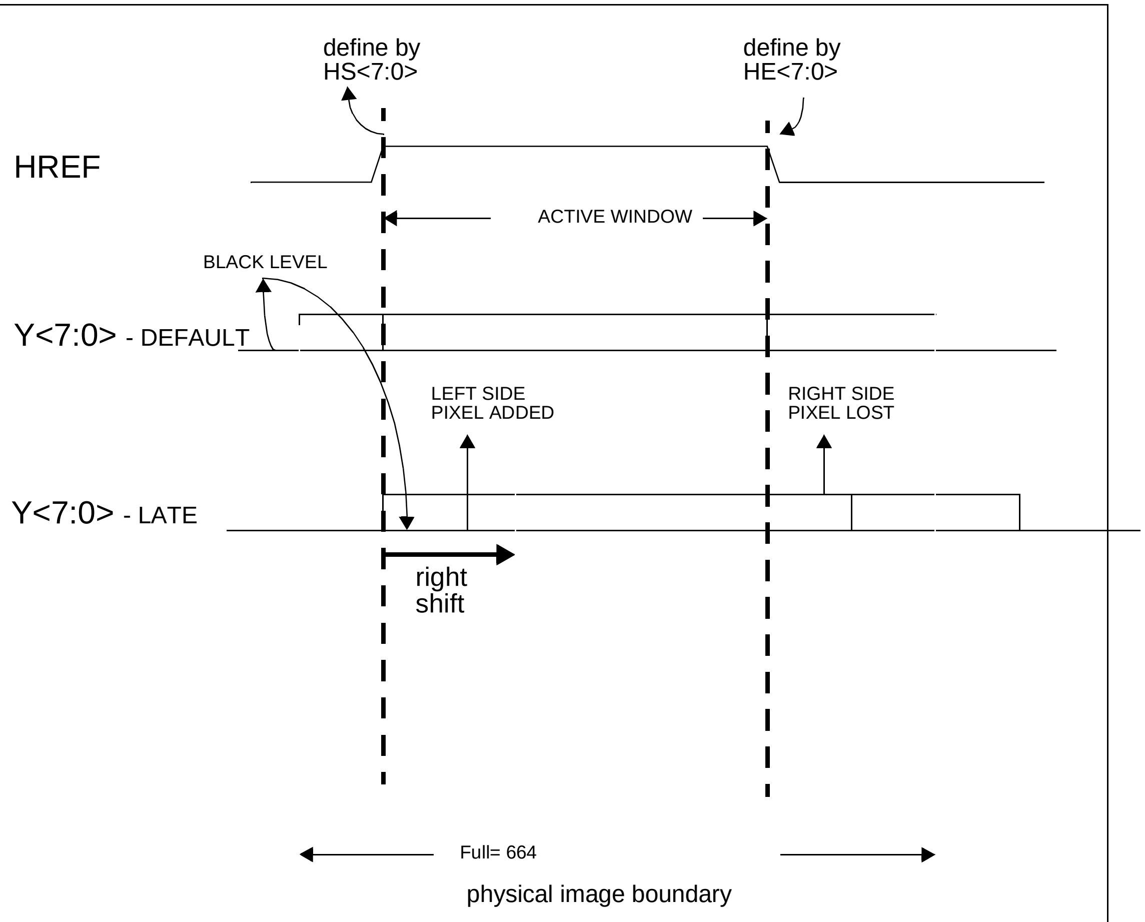


FIG 0.12 Pixel Shift Examples

Register 1C- r: Manufacture ID high byte

Bits	MIDH7	MIDH6	MIDH5	MIDH4	MIDH3	MIDH2	MIDH1	MIDH0
Default	0	1	1	1	1	1	1	1

MIDH<7:0> - read only, always returns “7F”.

Register 1D- r: Manufacture ID low byte

Bits	MIDL7	MIDL6	MIDL5	MIDL4	MIDL3	MIDL2	MIDL1	MIDL0
Default	1	0	1	0	0	0	1	0

MIDL<7:0>- read only, always returns “A2”

Register 1E ~ 1F- rw: Reserved

These two registers are reserved for internal use. Write data to these registers will not function.

Register 20- rw: Common control E

Bits	COME7	COME6	COME5	COME4	COME3	COME2	COME1	COME0
Default	0	0	0	0	0	-	0	0

COME7 - Modified CCIR656 format vertical sizing enabled. “1” will enable vertical windowing function. “0” will limit vertical size to 480 lines - unchanged by [19] and [1B].
COME6 - Field luminance average signal generation enable.Value is stored in register [7C]
COME5 - “1” First stage aperture correction enable. Correction strength will be decided by register [07]. “0” disable first stage aperture correction.
COME4 - “1” Second stage aperture correction enable. Correction strength and threshold value will be decided by register 26 bit 7 ~ register 26 bit 4.
COME3 - AWB smart mode enable. 1 - Drop out pixel when compare pixel red, blue and green component level to change register [01] and [02], which luminance level is higher than presetting level and lower than presetting level, this two level is set by register [0F]. 0 - calculate all pixels to get AWB result. Valid only when register 13 bit 0=1 and register 12 bit 2=1
COME2 - Reserved.
COME1 - AWB fast/slow mode selection. “1” - AWB is always fast mode, that is register [01] and [02] is changed every field/frame. “0” AWB is slow mode, [01] and [02] change every 16/64 field/frame decided by register 70 bit 1. When AWB enable, register 12 bit 2=1, AWB is working as fast mode at first 1024 field/frame, than as slow mode later.
COME0 - Digital output driver capability increase selection: “1” Double digital output driver current; “0” low output driver current status.

Register 21- rw: Y Channel Offset Adjustment

Bits	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Default	1	0	0	0	0	0	0	0

Y6-Y0: Y channel digital output offset adjustment. Range: +127mV ~ -127mV. If COMG2=0, this register will be updated by internal auto A/D BLC circuit, and write a value to this register with SCCB has no effect. If COMG2=1, Y channel offset adjustment will use the register stored value which can be changed by SCCB. If COMF1=0, this register has no adjustment effect to A/D output data. If output RGB raw data, this register will adjust R/G/B data.
Y7: Offset adjustment direction 0 - Add Y[6:0]; 1 - Subtract Y[6:0].

Register 22- rw: U Channel Offset Adjustment

Bits	U7	U6	U5	U4	U3	U2	U1	U0
Default	1	0	0	0	0	0	0	0

U6-U0: U channel digital output offset adjustment. Range: +128mV ~ -128mV. If register 27 bit 2=0, this register will be updated by internal auto A/D BLC circuit, and write a value to this register with SCCB has no effect. If register 27 bit 2=1, U channel offset adjustment will use the register stored value which can be changed by SCCB. If register 26 bit 1=1, this register has no effect to A/D output data. If output RGB raw data, this register will adjust R/G/B data.
U7: Offset adjustment direction: 0 - Add U[6:0]; 1 -Subtract U[6:0].
If register 2D bit 0 = 0, this register has no function.

Register 23- rw: Crystal Current control.

Bits	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
Default	0	0	0	-	-	-	-	-

CC7 - CC6: Crystal amplifier current gain. (00) maximum current; (11) minimum current
CC5 ~ CC0: Reserved

Register 24- rw: AEW Auto Exposure White Pixel Ratio

Bits	AEW7	AEW6	AEW5	AEW4	AEW3	AEW2	AEW1	AEW0
Interlace	0	0	0	0	1	0	0	0
Progressive Scan	0	0	0	1	0	0	0	0

Registers 24 and 25 together control the AEC target values for image brightness.
For a brighter image, increase register 24 and decrease register 25.
For a darker image, decrease register 24 and decrease reister 25.
AEW7-AEW0 - used to calculate the white pixel ratio. OV7620/OV7120 AEC algorithm counts the whole field/frame white pixel (its luminance level is higher than a fixed level) and black pixel (its luminance level is lower than a fixed level) number. When white/black pixel ratio is same as the ratio defined by registers [25] and [26], image stable. This register is used to define the white pixel ratio, default is 25%, each LSB represent step: Interlaced: 1.3%; Progressive Scan: 0.7%. Change range is: Interlaced: [01] ~ [4A]; Progressive Scan: [01] ~ [96]. Increase AEW<7:0> will increase the white pixel ratio. For same light condition, the image brightness will increase if AEW<7:0> increase.
Note: AEW<7:0> must combined with register [26] AEB<7:0>. Keep the relation always true: AEW<7:0> + AEB<7:0> > [4A] for Interlaced; AEW<7:0> + AEB<7:0> > [90].

Register 25- rw: AEC Auto Exposure Black Pixel Ratio

Bits	AEB7	AEB6	AEB5	AEB4	AEB3	AEB2	AEB1	AEB0
Interlace	0	1	0	0	1	0	1	0
Progressive Scan	1	0	0	0	1	0	1	0

AEB7-AEB0 - used to calculate the black pixel ratio. OV7620/OV7120 AEC algorithm is count whole field/ frame white pixel (its luminance level is higher than a fixed level) and black pixel (its luminance level is lower than a fixed level) number. When white/black pixel ratio is same as the ratio defined by registers [25] and [26], image stable. This register is used to define black pixel ratio, default is 75%, each LSB represent step: Interlaced: 1.3%; Progressive Scan: 0.7%. Change range is: Interlaced: [01] ~ [4A]; Progressive Scan: [01] ~ [96]. Increase AEB<7:0> will increase black pixel ratio. For same light condition, the image brightness will decrease if AEB<7:0> increase.

Note: AEB<7:0> must combined with register [25] AEW<7:0>. Keep the relation always true: AEW<7:0> + AEB<7:0> > [4D] for Interlaced; AEW<7:0> + AEB<7:0> > [90].

Register 26 - rw: Common control F

Bits	COMF7	COMF6	COMF5	COMF4	COMF3	COMF2	COMF1	COMF0
Default	1	0	1	0	0	0	1	0

COMF7 - COMF6: Digital Sharpness threshold selection.
[00] - Difference of neighbor pixel luminance is larger than 8 mV, correction on.
[01] - 16 mV.
[10] - 32 mV.
[11] - 64 mV.
COMF5 - COMF4: Digital Sharpness Magnitude selection.
[01] - Strength is 50% of difference of neighbor pixel luminance.
[10] - 100%.
[11] - 200%.
COMF3 - Reserved
COMF2 - Swap bus MSB/LSB. “1” LSB->Bit7, MSB->Bit0; “0” normal.
COMF1 - “1” A/D Black level calibration enable. Do not use “0”.
COMF0 - “1” Output first 4 line black level for Interlaced Mode and 8 line black level for Progressive Scan Mode before valid data output. HREF number will increase 4/8 relatively. “0” no black level output.

Register 27 - rw: Common control G

Bits	COMG7	COMG6	COMG5	COMG4	COMG3	COMG2	COMG1	COMG0
Default	1	1	1	0	0	0	1	0

COMG7: Reserved.
COMG6: Reserved.
COMG5: Reserved.
COMG4: RGB matrix disable. “1” - Bypass RGB matrix. “0” - Enable RGB matrix.
COMG3: Reserved.
COMG2: “1” Enables manual adjustment of A/D offset: 1 - A/D data will add or subtract a value defined by registers [21] and [22]. 0 - A/D data will be shifted by a value defined by registers [21], [22] and [2E], which is updated by internal circuit.
COMG1: - Disables CCIR range clip.
COMG0: - Special interface for external micro-controller and RAM timing control. See timing chart.

Register 28 - rw: Common control H

Bits	COMH7	COMH6	COMH5	COMH4	COMH3	COMH2	COMH1	COMH0
Default	0	0	0	0	0	0	0	0

COMH7: - “1” selects One-Line RGB raw data output format, “0” selects normal dual-line (repetitive) raw data output, effective only in Progressive Scan mode.
COMH6: - “1” enable Black/White mode.
COMH5: - “1” select Progressive Scan mode; “0” select Interlaced mode.
COMH4: - Freeze AEC/AGC value - current values retained. This is effective only when register 13 bit 0=1.
COMH3: - AGC disable.
COMH2: - Raw data output format: “1” - Green on Y channel, B R B R....on UV channel (GRB422), “0” - G R G R.... on Y channel, B G B G..... on UV channel.
COMH1: - 2x Gain boost. “1” Double PreAmp gain to 6dB. “0” PreAmp gain is 0dB.
COMH0: - Reserved.

Register 29 - rw: Common control I

Bits	COMI7	COMI6	COMI5	COMI4	COMI3	COMI2	COMI1	COMI0
Default	0	0	0	0	0	0	0	0

COMI7: - AEC disable. “1” If register 13 bit 0=1, AEC stop and register [10] value will be held at last AEC value and not be updated by internal circuit. “0” - if register 13 bit 0=1, register [10] value will be updated by internal circuit
COMI6: - Enable slave sync mode selection. “1” slave mode, use external CHSYNC and VSYNC. “0” master mode
COMI<5:4> - Reserved.
COMI3: - Central weighted exposure control.
COMI2: - Reserved.
COMI1 - COMI0: Version flag.

Register [2A] - rw: Frame Rate Adjust Register 1

Bits	EHSH7	EHSH6	EHSH5	EHSH4	EHSH3	EHSH2	EHSH1	EHSH0
Default	0	0	0	0	0	0	0	0

EHSH7 - Frame Rate adjustment enable bit. “1” Enable.
EHSH<6:5> - Highest 2 bit of frame rate adjust control byte. See explanation in register [2B].
EHSH4 - “1” - UV component delay 2 pixel. “ 0” no 2*Tp delay.
EHSH3 - Y channel brightness adjustment enable. When COMF2=1 active.
EHSH2 - For QVGA raw data format. “1” will force Y to output B G B G and UV to output G R G R
EHSH<1:0> - Reserved.

Register [2B] - rw: Frame Rate Adjust Register 2

Bits	EHSL7	EHSL6	EHSL5	EHSL4	EHSL3	EHSL2	EHSL1	EHSL0
Default	0	0	0	0	0	0	0	0

EHSL<7:0> - Lowest 8 bit of frame rate adjust control byte. Frame rate adjustment resolution is 0.12%. Control word is 10 bit. Every count decreases frame rate by 0.12%. Range is 0.12% - 112%. If frame rate adjustment is enabled, COME7 must be set to “0”.

Register [2C] - rw: Black Expanding Register

Bits	EXBK7	EXBK6	EXBK5	EXBK4	EXBK3	EXBK2	EXBK1	EXBK0
Default	1	0	0	0	1	0	0	0

EXBK<7:4> - Coarse Auto Black Level adjustment. Range is 0.08% - 1.3%
EXBK<3:0> - Fine Auto Black Level adjustment. Range is 0.08% - 1.3%.

Register [2D] - rw: Common Control J

Bits	COMJ7	COMJ6	COMJ5	OMJ4	COMJ3	COMJ2	COMJ1	COMJ0
Default	1	0	0	0	0	0	-	1

COMJ7 - Reserved. Always set to “1”.
COMJ6 - QVGA 60 frame/s selection. “1” Only Odd field in Interlace Mode data output, “0” Odd/Even field data output frame rate is 30 frames/s. VGA is output at 60 frames/s in dual line mode raw data.
COMJ5 - Reserved. Always set to “0”.
COMJ4 - Auto brightness enabled.
COMJ3 - Reserved. Always set to “0”.
COMJ2 - Banding filter enable. After adjust frame rate to match indoor light frequency, this bit enable a different exposure algorithm to cut light band induced by fluorescent light.
COMJ1 - Reserved. Always set to “0”.
COMJ0 - Reserved. Always set to “1”.

Register [2E]- rw: V Channel Offset Adjustment

Bits	V7	V6	V5	V4	V3	V2	V1	V0
Default	1	0	0	0	0	0	0	0

V7-V0: V channel digital output offset adjustment. Range: +128mV ~ -128mV. If COMG2=0, this register will be updated by internal auto A/D BLC circuit, and write a value to this register with SCCB has no effect. If COMG2=1, V channel offset adjustment will use the register stored value which can be changed by SCCB. If COMF1=1, this register has no effect to A/D output data. If output raw data, this register will adjust R/G/B data.
V7: Offset adjustment direction: o - Add V[6:0]; 0-Substrate V[6:0].
If COMJ0 = 0, this register value is common to U and V channel.

Register 2F ~ 5F - w: Reserved

Address [2F] - [5F] are reserved for internal use.

Register 60- rw: Signal Process Control A

Bits	SPCA7	SPCA6	SPCA5	SPCA4	SPCA3	SPCA2	SPCA1	SPCA0
Default	0	0	1	0	0	1	1	1

SPCA7: 1.5x gain boost.
SPCA6: Reserved.
SPCA5: “1” disables green averaging for UV channel.
SPCA4: “1” disables green averaging for lumninance channel.
SPCA<3:2> Reserved.
SPCA<1:0>: Reserved. Color set to “0111”; B&W set to “0000”.

Register 61- rw: Signal Process Control B

Bits	SPCB7	SPCB6	SPCB5	SPCB4	SPCB3	SPCB2	SPCB1	SPCB0
Default	1	0	0	0	0	0	1	0

SPCB7: “1” YUV mode; “0” raw data mode.
SPCB6: Reserved. Always set to “0”.
SPCB5: Reserved. Always set to “0”.
SPCB4: Reserved. Always set to “0”.
SPCB3: Reserved. Always set to “0”.
SPCB2: Limits range of register [6] to half value.
SPCB<1:0>: Auto Brightness target reference level: (00) -- 0 IRE; (01) -- 6 IRE; (10) -- 10 IRE; (11) -- 20 IRE.

Register 62- rw: RGB Gamma Control

Bits	RGM7	RGM6	RGM5	RGM4	RGM3	RGM2	RGM1	RGM0
Default	0	0	0	1	0	0	1	0

RGM<7:1> raw data or UV gamma curve selection.
RGM0: Reserved. Always set to “0”.

Register 63- rw: Reserved

Address [63] are reserved for internal use.

Register 64- rw: Y Gamma Control

Bits	YGM7	YGM6	YGM5	YGM4	YGM3	YGM2	YGM1	YGM0
Default	0	1	0	1	1	0	0	1

YGM<7:1>: Y gamma curve selection.
YGM<0>: “1” enable; “0” disable (linear).

Register 65- rw: Signal Process Control C

Bits	SPCC7	SPCC6	SPCC5	SPCC4	SPCC3	SPCC2	SPCC1	SPCC0
Default	0	1	0	0	0	0	1	0

SPCC<7:3> Reserved.
SPCC2: A/D mode selection. Increase A/D range by 1.5X
SPCC<1:0>: A/D reference selection. <00>: input signal range 0.9V; <01>: 1.0V peak
<10>: 1.15V peak; <11>: 1.26V peak. Do not use <00> selection.

Register 66- rw: AWB Process Control

Bits	AWBC7	AWBC6	AWBC5	AWBC4	AWBC3	AWBC2	AWBC1	AWBC0
Default	0	1	0	1	0	1	0	1

White balance limiting function - YUV matrix control.
Register 74:7 must be enabled for AWB process control.
AWBC<7:6>: Smart AWB ignores RGB raw data pixel values above (00):70%, (01): 80%, (10): 90%, (11):100%.
AWBC<5:4>: Smart AWB ignores RGB raw data pixel values below (00):10%, (01) 20%, (10) 30%, (11) 40%.
AWBC<3:2>: U threshold level selection if use U/V as white balance feedback
00: (-10% ~ 10%); 01: (-20% ~ 20%); 10: (-30% ~ 30%); 11: (-40% ~ 40%)
AWBC<1:0>: V threshold level selection if use U/V as white balance feedback
00: (-10% ~ 10%); 01: (-20% ~ 20%); 10: (-30% ~ 30%); 11: (-40% ~ 40%)

Register 67- rw: Color Space Selection

Bits	YUV7	YUV6	YUV5	YUV4	YUV3	YUV2	YUV1	YUV0
Default	0	0	0	1	1	0	1	0

YUV<7:6>: UV coefficient selection (U/V is output and u/v is input)

- [00]: YUV
- [01]: Analog YUV
- [10]: CCIR 601 YCrCb
- [11]: PAL YUV

YUV5: U/V signal delay 2 pixel selection
YUV4: U/V signal with 3 point chroma average(2 pixel delay accordingly)
YUV<3:2>: Y signal delay selection: (00) - 0; (01) - 1; (10) - 2; (11) - 3 pixels
YUV1: Auto saturation control (decreases color noise) enable.
YUV0: Auto saturation control range selection: 0 - 1.5x; 1 - 1x.

Register 68- rw: Signal Process Control D

Bits	SPCD7	SPCD6	SPCD5	SPCD4	SPCD3	SPCD2	SPCD1	SPCD0
Default	1	1	0	0	1	1	0	0

SPCD<7:5>: AEC/AGC Brighness Target level selection.
000 - 10%; 001 - 30%; 010 - 50%; 011 - 70%; 100 - 80%; 101 - 90%; 110 - 100%; 111 - 110%.
SPCD4: Reserved. Always set to “0”.
SPCD<3:2>: Anti-alias threshold: 11 lowest threshold; 01, 10 midrange threshold; 00 highest threshold.
SPCD<1:0>: Anti-alias magnitude: 00 - low strength; 01, 10 mid strength; 11:high strength.

Register 69- rw: Analog Sharpness

Bits	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0
Default	0	1	1	1	0	0	1	0

EDGE<7:3> Reserved.
EDGE2: Vertical Edge Enhancement enable. Register 20:5 must be set to “1”.
EDGE<1:0>: Reserved.

Register 6A- rw: Vertical Edge Enhancement Control

Bits	VEG7	VEG6	VEG5	VEG4	VEG3	VEG2	VEG1	VEG0
Default	-	1	0	0	0	0	1	0

VEG<6:4>: Vertical Edge Enhancement threshold range
VEG<3:0>: Vertical Edge Enhancement magnitude value. 0000: weakest; 1111: strongest.

Register 6B-6E rw: Reserved

Address [6B] - [6E] are reserved for internal use.

Register 6F - rw: Even/Odd Noise Compensation Control

Bits	EOC7	EOC6	EOC5	EOC4	EOC3	EOC2	EOC1	EOC0
Default	-	-	1	1	1	0	1	0

EOC<7:6>: Reserved.
EOC<5:4>: Color Kill luminance threshold selection: 00 - none; 01 - 2.6v; 10 - 2.4v; 11 - 2.3v. Lower luminance selection will activate color kill.
EOC<3:0>: Set to factory recomended values.

Register 70 - rw: Common Control K

Bits	COMK7	COMK6	COMK5	COMK4	COMK3	COMK2	COMK1	COMK0
Default	1	0	0	0	0	0	0	1

COMK7 - “1” HREF edges coincident (no delay) with PCLK negative/falling edges (COMD6 must be set to “0”). “0” HREF edge occurs 10 ns after PCLK positive/rising edge.
COMK6 - Output port drive current additional 2x control bit.
COMK5 - Reserved.
COMK4 - Selects ZV port timing. “1” VSYNC output ZV port vertical sync signal. “0” normal TV vertical sync signal.
COMK3 - Accelerated saturation mode for camera mode change. (QVGA, 8 Bit output, CCIR 656 mode and Progressive Scan Mode). After relative control bit set, the first VS will be the stable image with suitable AEC/AWB setting. “0” - slow mode, after mode change need more field/frame to get stable AEC/AWB setting image.
COMK2 - Reserved.
COMK1 - AWB update rate selection. “1” fast mode; “0” slow mode.
COMK0 - Set to “1” in single line mode, otherwise set to “0” and set COMG4 to disable.

Register 71 - rw: Common Control J

Bits	COML7	COML6	COML5	COML4	COML3	COMK2	COML1	COML0
Default	0	0	0	0	0	0	0	0

COML7 - Auto Brightness update rate: “1” - Slow mode; “0” - fast mode.
COML6 - Gated PCLK selection. “1” - Enables PCLK gated by HREF; “0” - PCLK is free running clock
COML5 - Swap HREF output pin with CHSYNC. “1” - HREF pin output CHSYNC signal; “0” - No swap.
COML4 - Swap CHSYNC output pin with HREF. “1” - CHSYNC pin output HREF signal; “0” - normal output.
COML<3:2>- Highest 2 bit for HSYNC rising edge shift control, combined with register [72]
COML<1:0>- Highest 2 bit for HSYNC falling edge shift control, combined with register [73]

Register 72- rw: Horizontal Sync 1st Edge shifting

Bits	HSDY7	HSDY6	HSDy5	HSDY4	HSDY3	HSDY2	HSDY1	HSDY0
Default	0	0	0	1	0	1	0	0

HSDY<7:0> - Lower 8 bit control for shifting horizontal sync CHSYNC first edge. Range is [000] - [3FF]. Every count equals 1 PCLK.

Register 73 - rw: Horizontal Sync 2nd Edge shifting

Bits	HEDY7	HEDY6	HEDY5	HEDY4	HEDY3	HEDY2	HEDY1	HEDY0
Default	0	1	0	1	0	1	0	0

HSDY<7:0> - Lower 8 bit control for shifting horizontal sync CHSYNC second edge. Range is [000] - [3FF]. Every count equals 1 PCLK.

Register 74 - rw: Common Control M

Bits	COMM7	COMM6	COMM5	COMM4	COMM3	COMM2	COMM1	COMM0
Default	0	0	1	0	0	0	0	0

COMM7 - Enable UV Smart AWB threshold control.
COMM<6:5> - AGC maximum gain selection: 00 - 2x; 01 - 4x; 10 - 2x; 11 - 8x
COMM<4:0> - Reserved.

Register 75 - rw: Common Control N

Bits	COMN7	COMN6	COMN5	COMN4	COMN3	COMN2	COMN1	COMN0
Default	1	0	0	0	0	0	1	0

COMN7 - “1” enables Auto brightness range limit. Minimum will be [40]. Otherwise will be [00] ~ [FF].
COMN<6:3> - Reserved.
COMN2 - This bit further reduces the exposure time to 1/120 second or 1/100 second when the banding filter is enabled and the light is too strong.
COMN1- If enabled, manual write white balance value, then change to auto, the stable time will be less. Speeds white balance stable time when switching from manual to AWB.
COMN0 - Enables addition of 2 pixel averaging.

Register 76 - rw: Common Control O

Bits	COMO7	COMO6	COMO5	COMO4	COMO3	COMO2	COMO1	COMO0
Default	0	0	0	0	0	0	0	0

COMO7 - Output XCLK from **FODD** pin.
COMO6 - Reserved.
COMO5 - Software power down enable: 1 - enable; 0 - wake up
COMO4 - Reserved.
COMO3 - Limits the Minimum Exposure time to 4 lines rather 1 line with AEC enable
COMO2 - Tri-state sync and CLK output, except data line
COMO<1:0> - Reserved.

Register 77-7B - rw: Reserved

Address [2F] - [5F] are reserved for internal use.

Register 7C - rw: Field Average Level Storage

Bits	AVG7	AVG6	AVG5	AVG4	AVG3	AVG2	AVG1	AVG0
Default	0	0	0	0	0	0	0	0

AVG<7:0> -- Strorage fileld luminance average value if register 20 bit 6=1.
Notice: for QVGA and Progressive Scan mode, the real luminance average value is double of this register value, other mode is same. If set to RGB raw data mode, the value is Green component average value.

SECTION 1 PIN DESCRIPTION

1.1 PINOUT

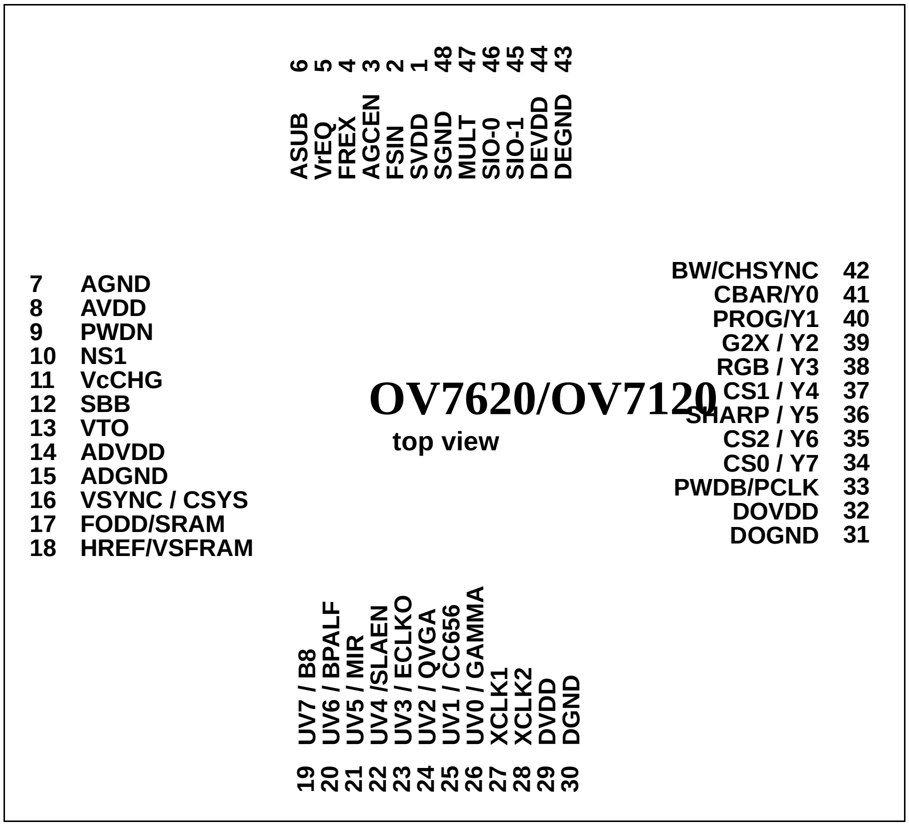


FIG 1.1 OV7620/OV7120 48Pin Digital Package

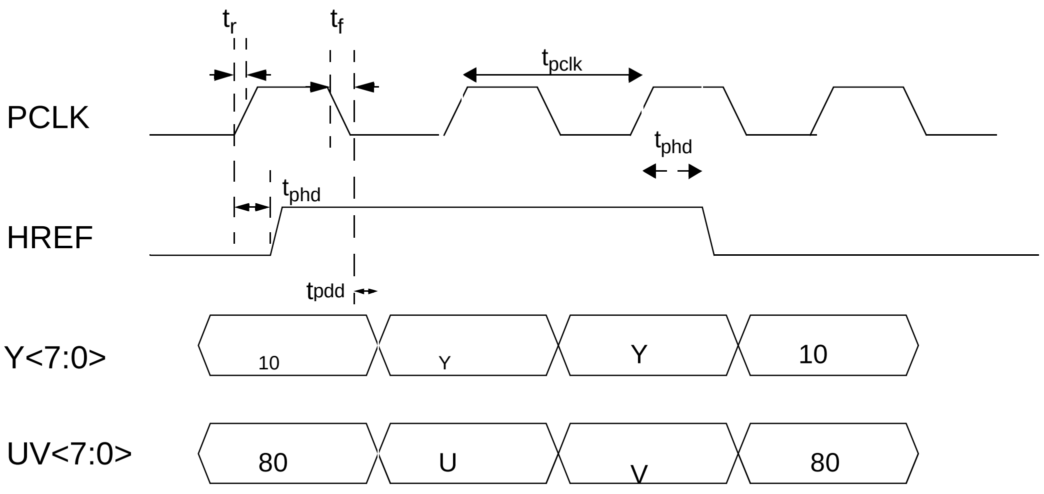


FIG 1.2 Pixel Timing

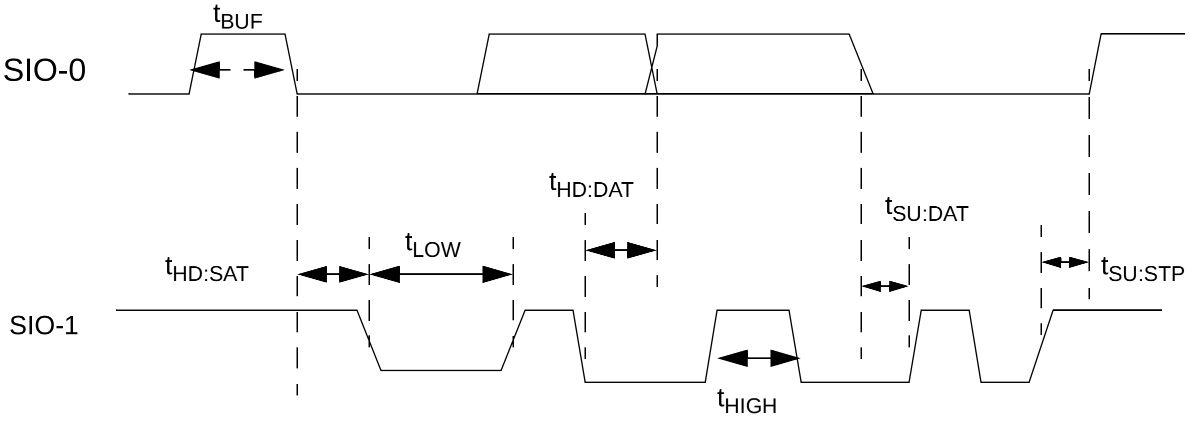
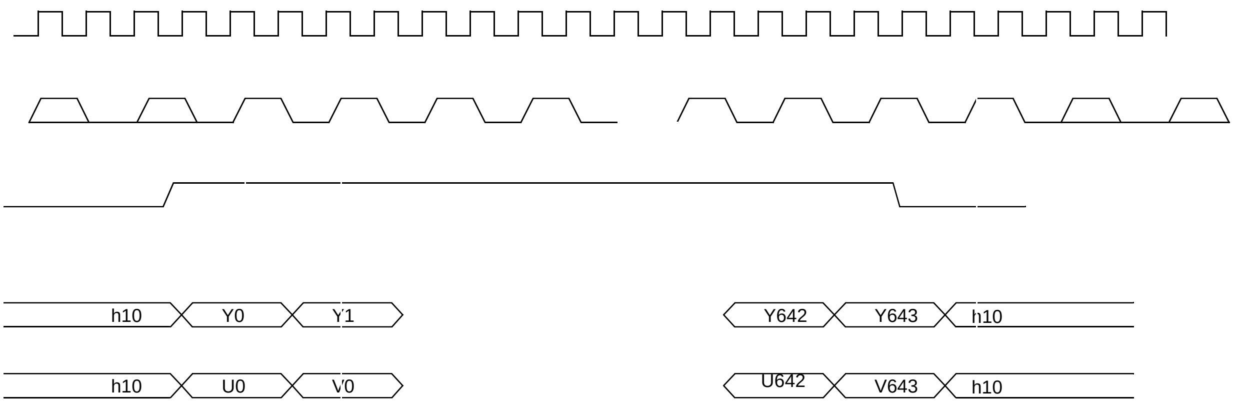
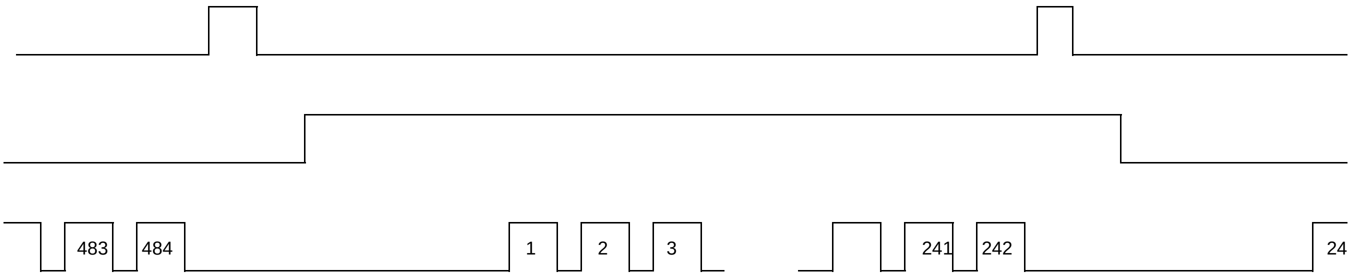


FIG 1.3 SCCB Bus Timing

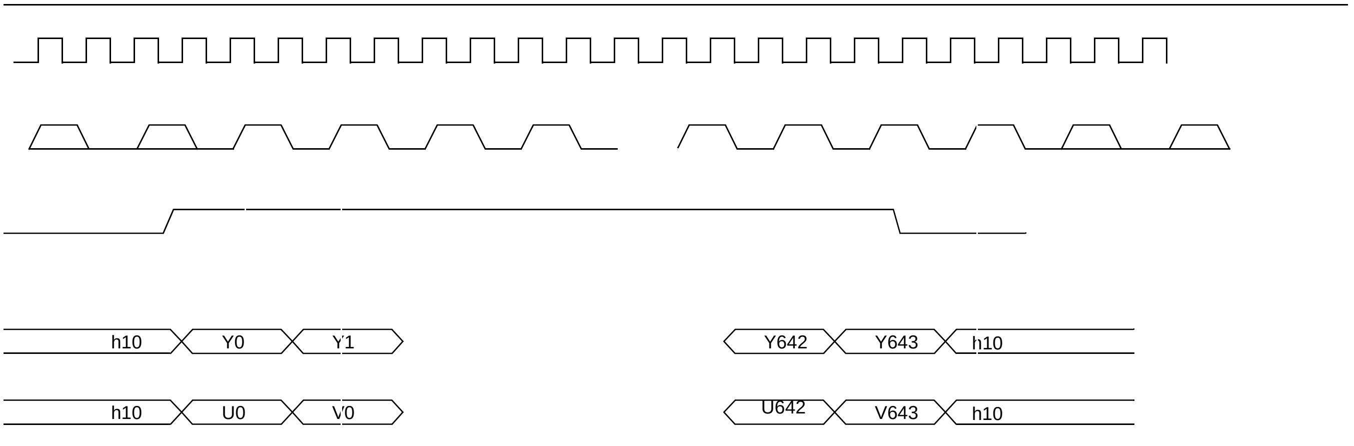


(a) HORIZONTAL TIMING

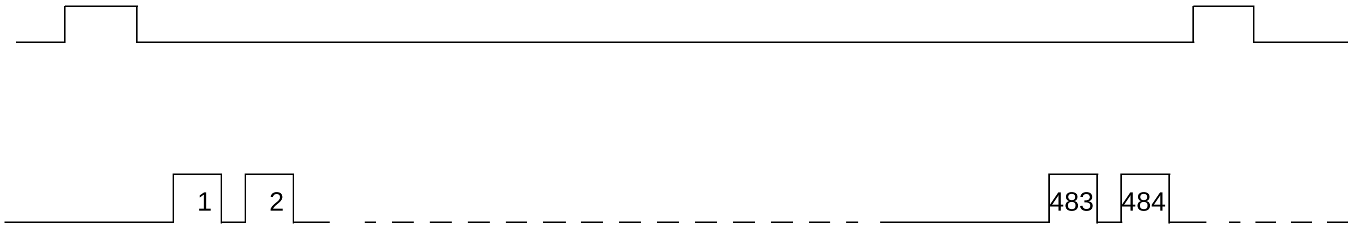


(b) VERTICAL TIMING (Interlaced Mode)

FIG 1.4 16 Bit 4:2:2 Video Port Timing (Interlaced Mode)



(a) HORIZONTAL TIMING



(b) VERTICAL TIMING (Progressive Scan Mode)

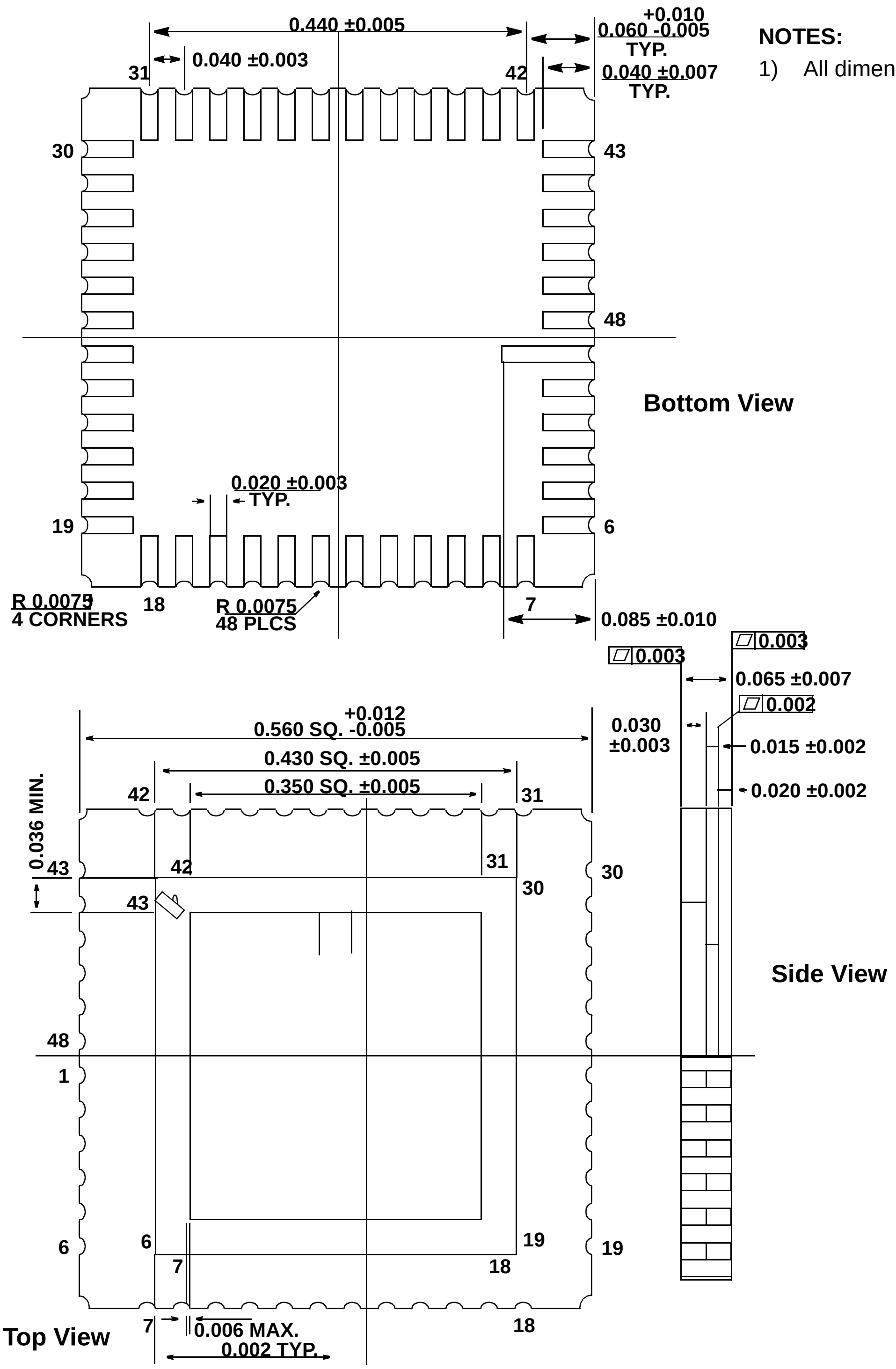
FIG 1.5 16 Bit 4:2:2 Video Port Timing (Progressive Scan Mode)

3. Different Method to get QVGA format Compare

Table 1.11: Compare of QVGA Method

Method	Resolution	Frame Rate	Lens
A	320x240	60 frame/s	1/3”
B	320x240	30 frame/s	1/3”
C	322x240	30 frame/s	1/4”
D	354x288	30 frame/s	1/4”

Note: To get the frame rate, OV7620/OV7120 must use 27 MHz crystal.



NOTES:

1) All dimensions in inches

FIG 1.6 Package Mechanical Data

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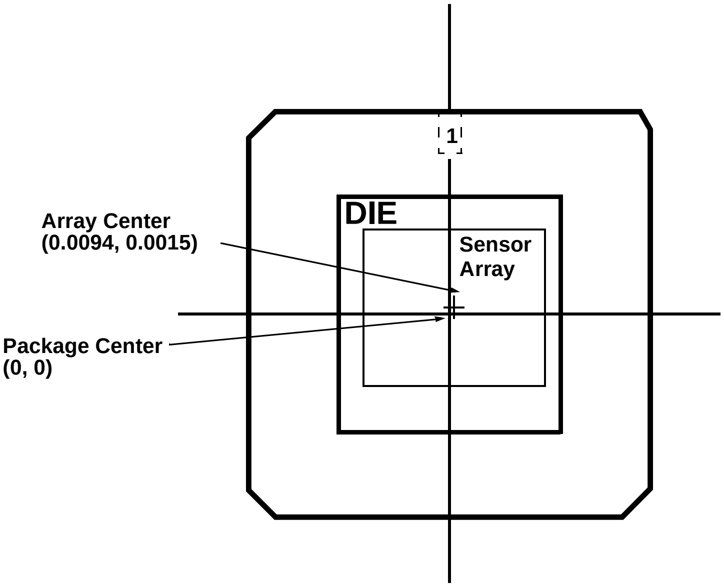

Top View

FIG 1.7 OV7620 Sensor Array Location (in inches)

Ordering Information

Part Number	Description	Comments
OV7620	Color Digital Sensor	48 pin LCC